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ELECTRONIC DESIGN

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OCTOBER 3, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

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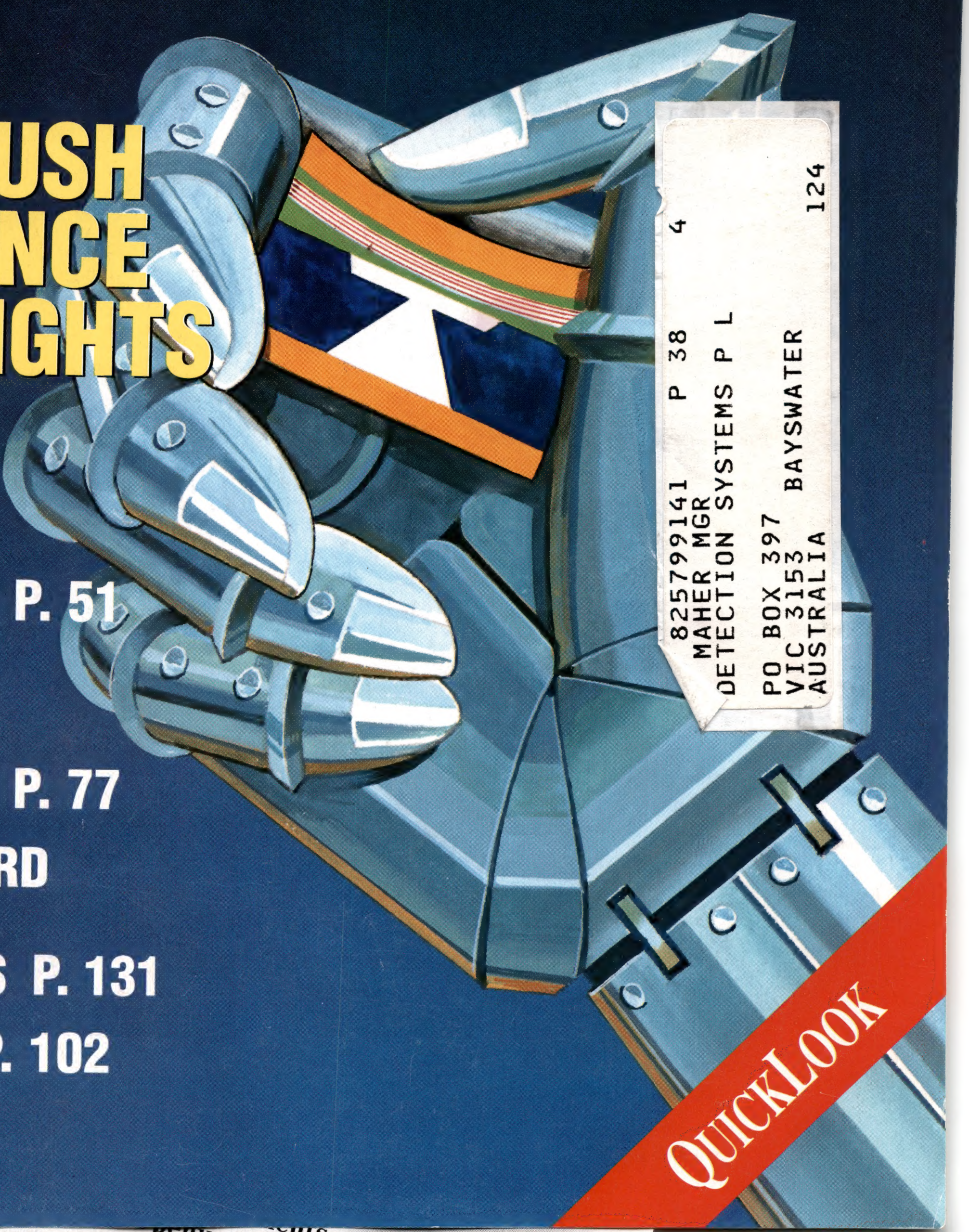

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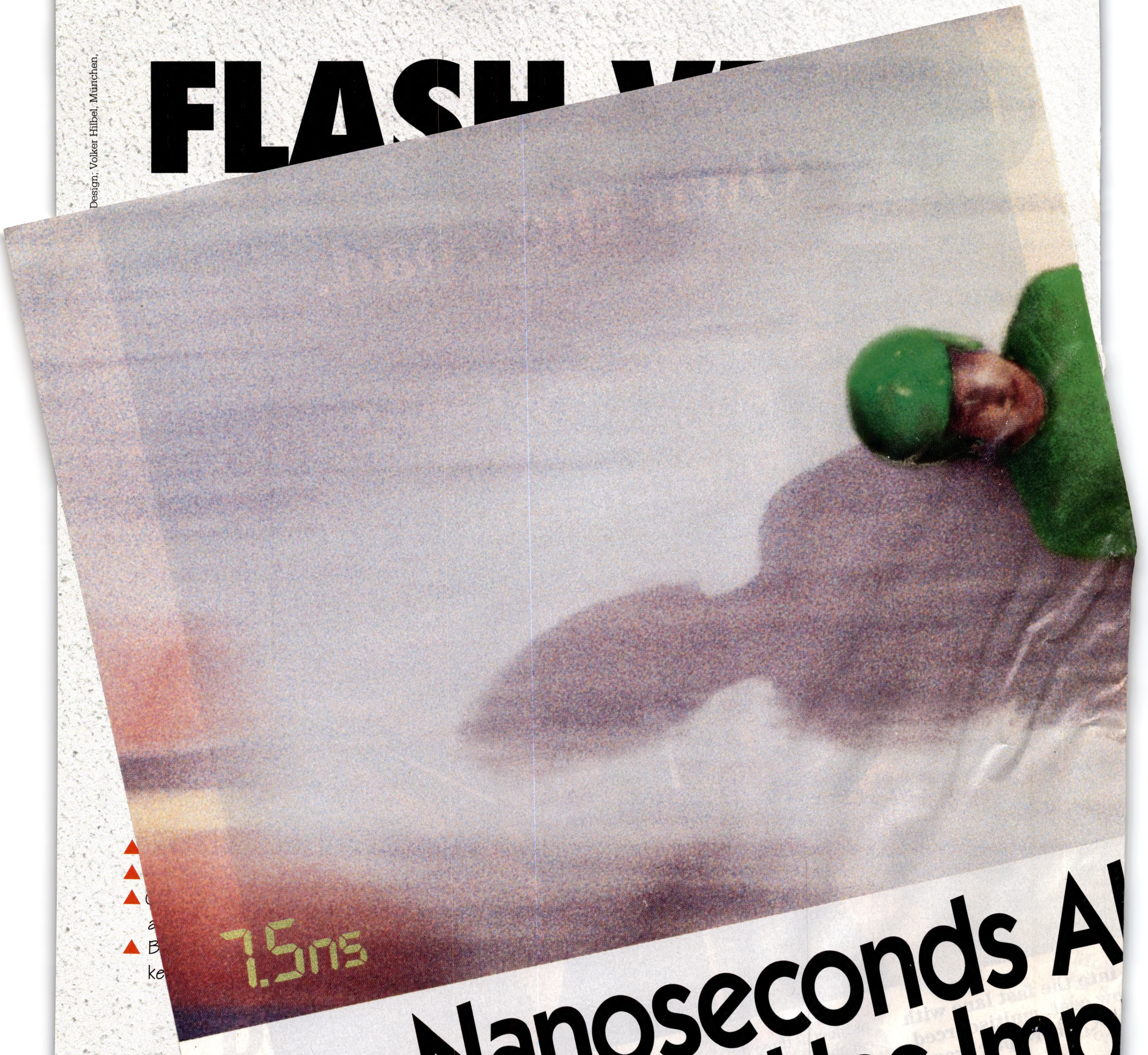

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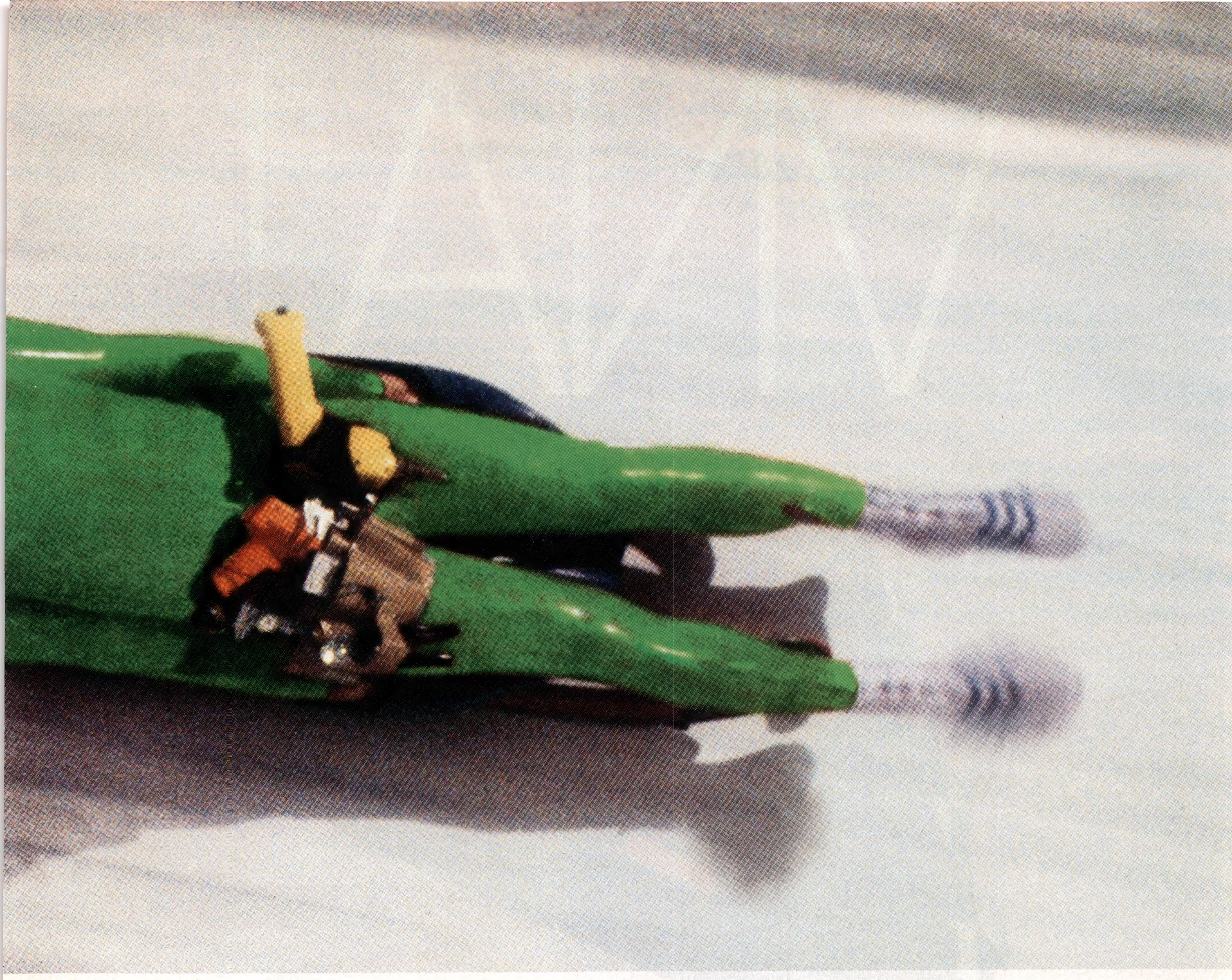

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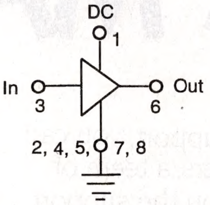

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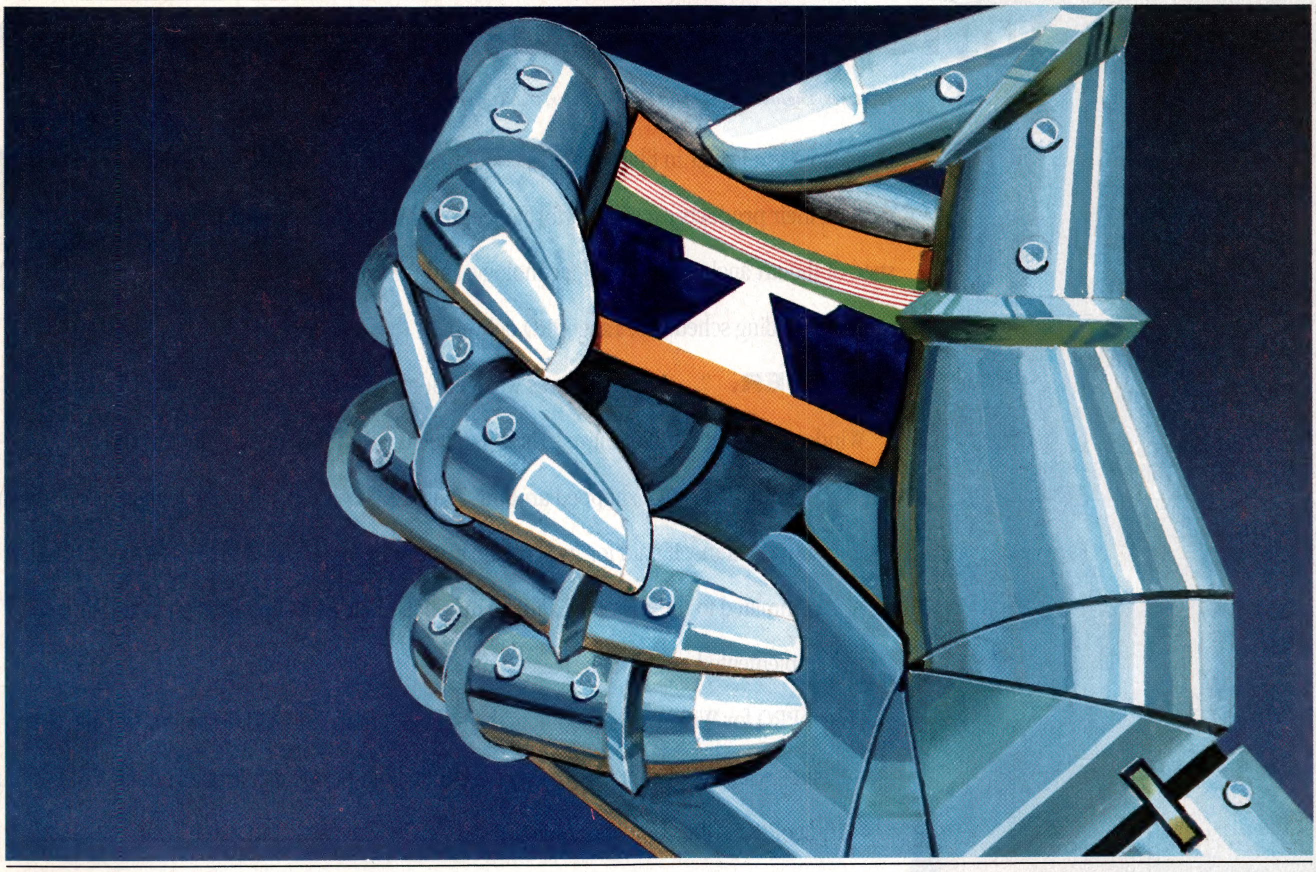

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- Why VXIbus is becoming more user-friendly
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- Low-cost method of implementing Fibre Channel
- PLUS:
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ELECTRONIC DESIGN 40 YEARS AGO

New Literature: Tube Manual

A revised edition of the RCA Receiving Tube Manual provides basic technical data on over 500 receiving-type electron tubes used in radio, television, and sound equipment. The manual (RC-17) features 67 new tube types, including the company's tricolor kinescope. Pertinent technical information for each of the tubes in the book is amplified by outline drawings, socket diagrams, and characteristic curves. The manual also provides new hi-fi amplifier circuits, a receiving tube classification chart, a kinescope characteristics chart with indexed kinescope data, and socket information and phosphor curves. It further includes a listing of the most important obsolete tube types with technical data important to service technicians, and revised and expanded text material which describes cathode drive circuits and the effect of contact potential on tube performance. Price of the manual is 60 cents. Write to Commercial Engineering, RCA Tube Division, Harrison, N.J. *(Electronic Design, October 1954, p. 96.)*

Few engineers did without a personal copy of a tube manual, if for nothing else than as an aid in troubleshooting their TV sets at home. And, with the resurgence of interest in high-quality vacuum-tube audio amplifiers and the increasingly popular trend of restoring old radios and TV sets, such manuals might even become more valuable.—SS

New Literature: Buying Guide

Everything in electronic devices from transistors to consumer goods is listed in this 306-page, paper-bound catalog. This distributor supplies components to the industrial market from stock. In addition to transistors, germanium, selenium, and silicon diodes of all manufacturers are listed with prices. The catalog is particularly useful to designers who require components quickly or who require samples of a particular type of component in order to select the best product for their needs. Allied Radio Corporation, Dept. ED, 100 N. Western Ave., Chicago 80, Ill. *(Electronic Design, October 1954, p. 96.)*

By 1954, transistors and semiconductor diodes already had moved into the distribution channels. And, like the RCA Tube Manual, the Allied Radio catalog (or something similar from another parts distributor) was a fixture in most engineers' home workshops. Many electronics tinkerers got their start with mail-order parts from Allied.—SS

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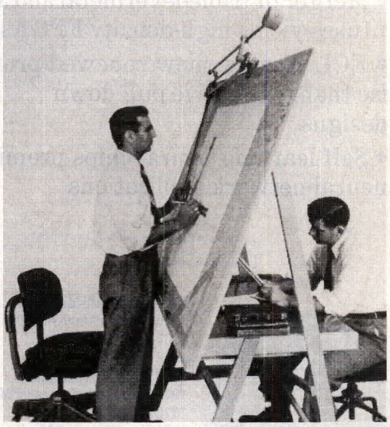

Many engineers began their careers at a drawing board. Now, the board, along with the T square, triangles, pencils of various hardness, sharpeners, erasers, erasing shields, french curves, tacks, tack lifters, templates, and similar paraphernalia have been supplanted by the mouse and keyboard.—SS

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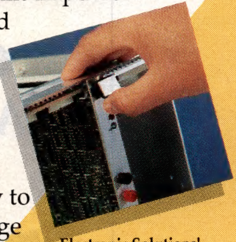

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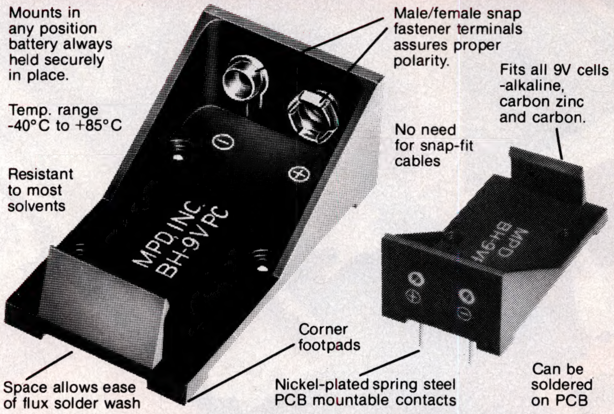
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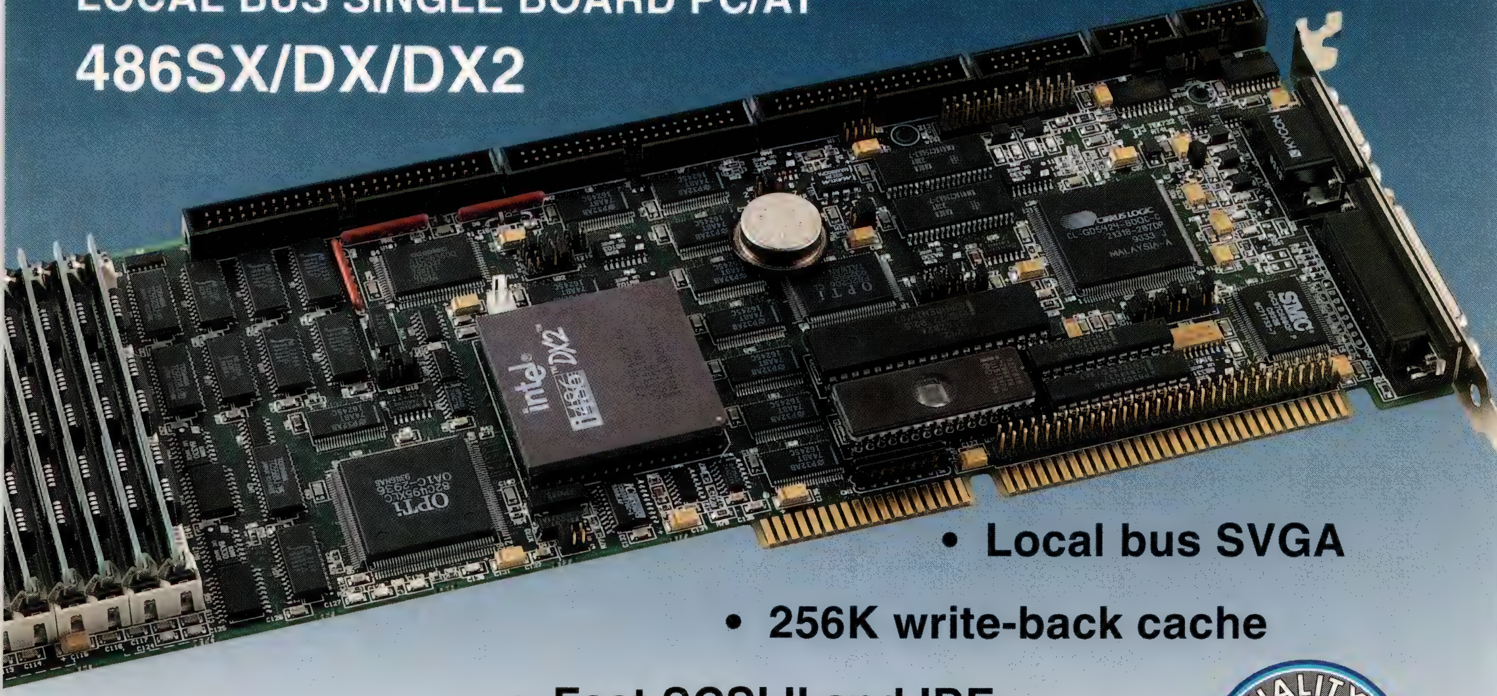

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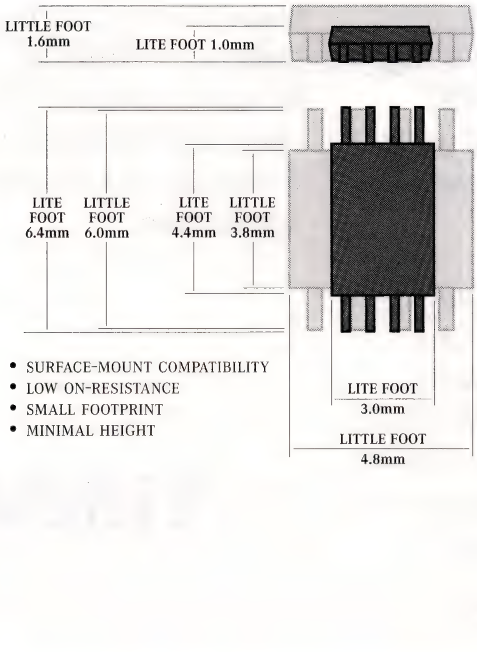

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LITE FOOT Part No.	TYPE	V_{DS} (V)	$r_{DS(on)}$ (mΩ)*	I_A (A)
Si6436DQ	Single N-Ch	30	50	4.2
Si6956DQ	Dual N-Ch	20	100	2.5
Si6433DQ	Single P-Ch	-12	75	3.5
Si6447DQ	Single P-Ch	-20	100	3.0
Si6953DQ	Dual P-Ch	-20	200	1.7
Si6542DQ	Complementary			
	N-Ch	20	100	2.5
	P-Ch	-20	200	1.7

* On-Resistance shown at V_{GS} = 10 V, except Si6433DQ shown at V_{GS} = 4.5 V

MOSFET thin enough to fit into any standard PCMCIA card. Even double-sided circuit boards are a snap.

What's more, LITE FOOT's mini package maximizes power dissipation, too – over 1.5 W in a tiny 8-lead TSSOP. But best of all, you don't need an external heat sink other than the PC board itself.

So if your designs keep shrinking, but your power management needs keep getting bigger, LITE FOOT is the solution.

Contact your local TEMIC sales office, or call **1-800-554-5565, ext. 531** for a LITE FOOT design guide.

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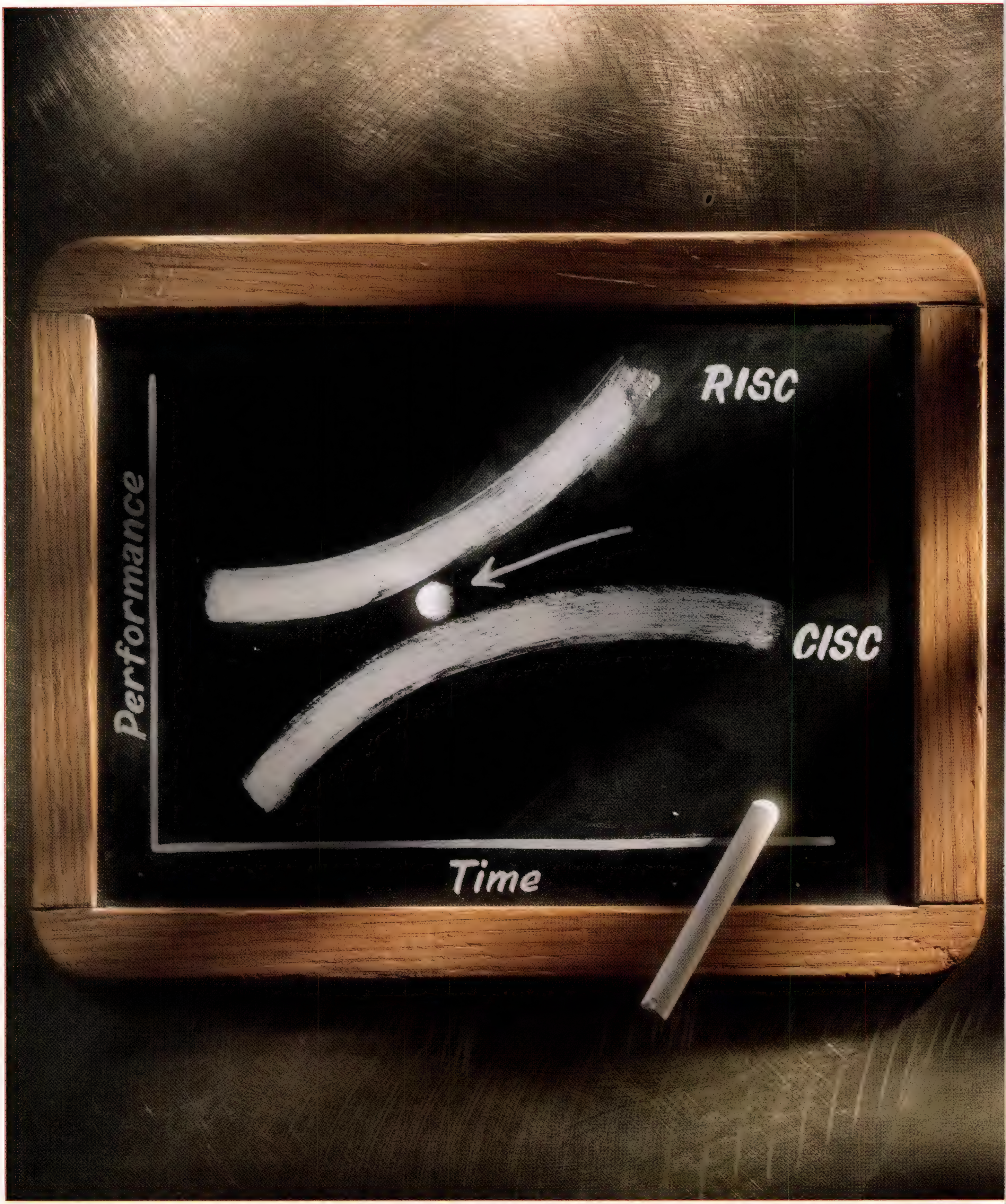

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At a certain point, everyone understands the benefits of RISC over CISC.

In the debate over which microprocessor technology is best for today's emerging computing needs, there's one point on which everyone can agree.

It's the one in the middle of the chart to your left. And what it illustrates is that, over time, microprocessors powered by RISC technology will outperform those driven by 15-year-old CISC architecture.

Update

◆

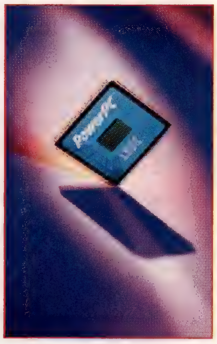
In July, we shipped our one millionth PowerPC 601 microprocessor, after just ten months of production.

That's vital news for everyone who makes or uses personal computers. Because the fact is, it takes the extraordinary processing power of RISC chips like our PowerPC™ family to drive today's and tomorrow's leading-edge computers and software. Which makes possible such innovative applications as realtime voice dictation, wireless networks, voice and handwriting recognition, and full-screen, full-motion multimedia, to name a few.

Some of these startling capabilities are already at work in advanced PCs and workstations. Two acclaimed examples are IBM's RISC System/6000™ workstation and Apple's Power Macintosh™ series, both powered by our PowerPC 601.™ Smaller, faster and less expensive to produce than non-RISC chips, the 601 makes it possible for these systems to run faster than CISC-based models, yet cost roughly the same.

Of course, all these advantages are hardly accidental. The fact is, because RISC (Reduced Instruction Set Computing) processors carry only the most frequently used instructions, they offer streamlined performance levels that CISC (Complex Instruction Set Computing) chips simply can't match. Specifically, the simpler instructions implemented in RISC processors are typically executed in one system clock cycle, while CISC instructions often take five or even fifty system clock cycles to execute. The result is that the average number of system clock cycles per instruction in RISC typically eliminates advantages touted by CISC manufacturers.

And the best is yet to come. Since RISC-based PowerPC chips are built with IBM superscalar technology, we can all look forward to even greater performance benefits down the road. Right this minute, in fact, systems from palmtops to high-end workstations are under development utilizing IBM's PowerPC 603™, PowerPC 604™ and PowerPC 620™.



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DISINFORMATION

It looks as though the industry is gearing up for still another round of microprocessor wars. As product cycle times (except for software) spiral downward, the crowning of a preeminent microprocessor architecture is turning into an ongoing event. I'm not speaking of market-share leaders, of course. That will continue to be the 80X86 architecture for some time to come, simply because of the installed base of software applications.

From a strictly technological point of view, however, the leadership mantle is up for grabs at any moment in time, or so it seems, and probably will remain that way through the rest of the decade. There will always be a current favorite, just as the PowerPC is now and perhaps Digital Equipment's Alpha before that and Sun Microsystems' Sparc before that.

In the electronics industry, microprocessor watching is one of our favorite industry pastimes. Microprocessors are crucially important to the industry, but microprocessor watching also is a leisure activity—something akin to talking baseball or politics. Everybody has his or her favorite and the choice is largely a matter of personal preference.

And just as there are big bucks at stake in baseball and politics, there's a pile of gold at stake in microprocessors. Just ask Intel. This is something I always keep in mind as I try to decipher the pronouncements coming out of the competing camps. For example, I have to decide what is true and what is disinformation.

Just as politicians and major-league baseball owners divulge information calculated to lead the listener in the wrong direction, the folks quoting specs and describing architectures might very well be throwing in some misleading details here and there. The difference, of course, is that information divulged at a technical conference is (and should be) held in higher regard than statements made at news conferences. As someone who isn't anywhere close to being a microprocessor architect, I have to rely on third parties, and even they can be wrong.

Does the future belong to VLIW (very-long-instruction-word) architectures, such as those reportedly being pursued by Intel and Hewlett-Packard, or will boosting clock frequencies into the stratosphere provide the engine for the golden age of computing? Or will it be something else? Only time will tell. Certainly, the press releases won't.

Jack Shandle

Editor-in-Chief

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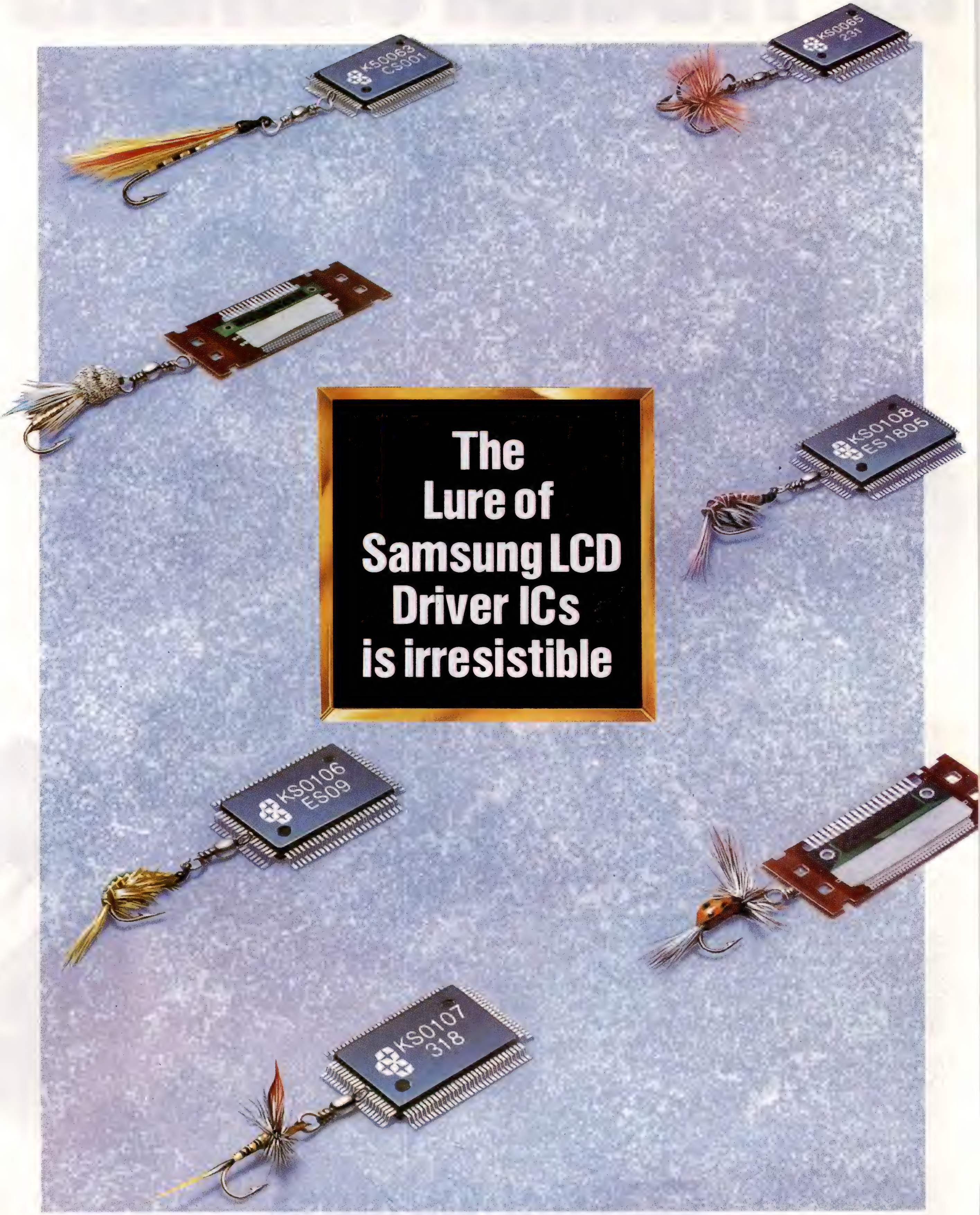
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Character	KS0063	80seg DR	100QFP	5	11		NOW
	KS0076	16C/40S CNTR & DR	80QFP	3/5	5		NOW
	KS0068	16C/60S CNTR & DR	100QFP	5	10		NOW
	KS0070	16C/80S CNTR & DR	128QFP	3/5	10		NOW
	KS0071	32C/60S CNTR & DR	128QFP	3/5	13.5		94.4Q
Graphic with RAM	KS0107	64com DR	100QFP	5	17	600K	NOW
	KS0108	64seg DR	100QFP	5	17	1.0M	NOW
Graphic	KS0083	80com/seg	100QFP	−5	28	3.3M	NOW
	KS0084	80com/seg Mirror	100QFP	−5	28	3.3M	94.2Q
	KS0786	80seg DR	98STAB	3/5	33	6.5/8M	94.4Q
	KS0787	160seg DR	191STAB	3/5	37	6.5/8M	94.4Q
	KS0788	160com/seg DR	197STAB	3/5	40	8/12M	94.4Q
	KS0789	100com DR	120STAB	3/5	38	1M	94.4Q
TFT for TV	KS0601	120gate	135STAB	5	30	50K	NOW
	KS0602	120source	141STAB	5	18	10M	NOW
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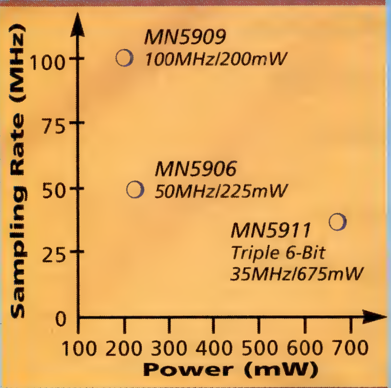

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WHY CAN'T WE ALL JUST GET ALONG?

The long plane flight home left me exhausted. Shock and numbness kept me from realizing how much covering the latest siege had affected me, until I saw Catherine's face as she met me at the door. She got me something cold and we sat quietly on the porch in the deepening colors of the approaching evening.

"It's bad?" inquired Catherine, finally breaking the silence. "The usual," I replied, "but worse this time. I just can't get the faces of those refugees out of my mind, all those engineers and MIS managers fleeing from the market when the shooting started. So many left homeless, wounded, or worse. All over a stupid piece of market share."

The LAN wars have been around for a long time. It started as an internal political struggle, with several factions pushing for star configurations and other simple remedies to feed the bandwidth-starved population. Then, a breakaway faction declared the ATM manifesto in an attempt to bring equality between data, voice, and video. This notion galvanized a vocal minority of the population who organized a carefully engineered coalition which seemed to be gaining popular support in the less strongly controlled hamlets at the fringes of the WAN.

LEE GOLDBERG
COMMUNICATIONS

Once news of insurrection reached the ruling powers, retribution was swift and fierce. Fundamentalist theologians railed against the danger of embracing unorthodox technologies, while the leaders promised LAN reform. In the process of rolling out the big guns to crush the ATM insurrection, two generals from different camps began to fight about which technology would lead the charge and began to shell each other.

From that point, it became a free-for-all, with splinter groups and minor warlords arriving on the scene and staking out their own small territories. The choices for the non-combatants were grim at best. Some fled to the fortress, where the ruling powers were entrenched and endured a relentless shelling from the angry mob outside. Others cast their lot with one of the rebel factions, sometimes by choice—sometimes by coercion.

As I left this latest trade show, a large portion of the populace appeared dispossessed, stumbling about in shell-shock, looking for a way out. Sitting here, safely in my cubicle, I can still smell the aroma of burning standards and the faces of panic-stricken MIS managers fleeing the WAN, with no safe haven.

This is not the first civil war I have covered. In the past year, we have witnessed the balkanization of the cellular telephone empire, vicious fratricide within computer telephony, and the raging broadband WAN wars, which threaten to pit the phone companies, cable companies, and even the damn electric companies in a bloody conflict for the right to pipe 328 channels of home shopping into the glazed eyeballs of the American family.

Sure, any significant change to the status quo will bring its attendant share of conflicts as the power structure re-arranges itself, but this is ridiculous. I would hate to be an engineer or MIS manager these days, trying to figure out whether the next technology I committed to would be out of favor before my project ever even got out the door. I'm not against innovation, it's just that technological advances find it much harder to gain a foothold when their market is highly fractured. All of us need to think just a little bit about what would be good for our customers and the industry as a whole before going off and starting another civil war.

While politics and economics have always played a significant role in shaping which technologies dominate, and how they are used, the huge potential profits in the communication market have created an even more contentious environment than usual. If not for the sake of our customers or the industry, then for our own sakes, let's try to work together on some of the big issues. Otherwise, we may end up burning down the very neighborhood we are trying to protect.

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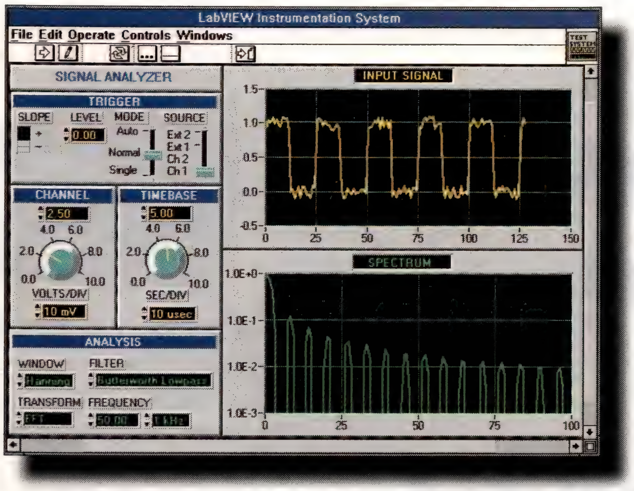

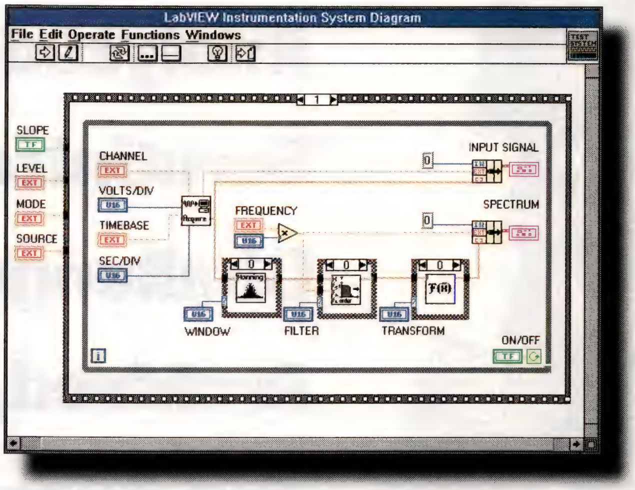

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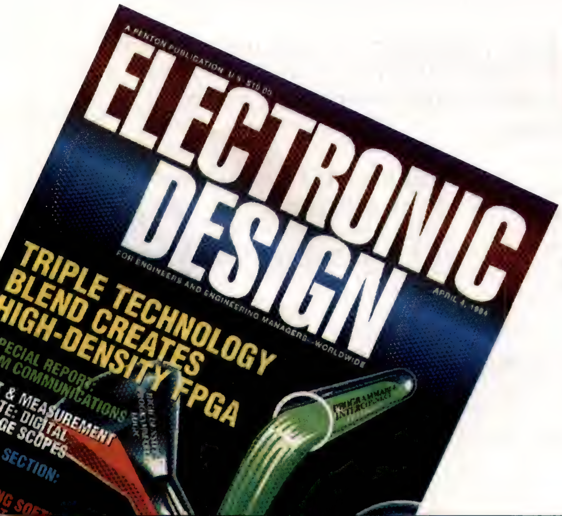

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TECHNOLOGY NEWSLETTER

JOINT OPTOELECTRONICS AGREEMENT NOW IN PLACE

The United States and Japan have agreed on the last critical step before realization of a joint program to further the design and development of advanced computing technologies that integrate optical and electronic components. The agreement was reached at a recent meeting between two Japanese organizations—the Ministry of International Trade and Industry and the Real World Computing Partnership—and five U.S. agencies. It establishes the process for funding a "broker," through which the Joint Optoelectronics Project will be carried out in the U.S. The broker is a service that links designers of advanced computer systems dependent on optoelectronic devices and modules with suppliers of such components in research and development divisions of companies in both countries. Each country will have its own broker, but suppliers in both nations will be available to Japanese and American designers.

According to the agreement, the National Institute of Standards and Technology (NIST) will oversee the selection of the broker in the United States to be funded by the Real World Computing Partnership. The two brokers will bring together designers of innovative, advanced computer systems and fabricators of optoelectronic components, allowing designers to evaluate their ideas by manufacturing experimental prototypes. For more information, contact Anne Enright Shepherd at (301) 975-4858. *CA*

INTEROPERABILITY PUT TO THE TEST

A group of computer-networking equipment makers have shown that the Integrated Services Digital Network could be used to link their products and provide communication between diverse applications. The multi-company hookup used the Point-to-Point Protocol running over an ISDN basic-rate-interface B-channel to demonstrate interoperable, local- and wide-area-network connectivity at a recent meeting of the North American ISDN Users' Forum (NIUF). As part of the demonstration, vendors and end users accessed Internet, read their electronic mail, and sent files back home.

Interoperability, a key component of the National Information Infrastructure, will enable rapid expansion of telecommuting, remote Internet access, and connection with branch offices. Seven vendors from the U.S., Canada, and Europe participated in the demonstration: AccessWorks Communications, Cisco Systems, DigiBoard, Gandalf Technologies, IBM Corp., netCS Informationstechnik, and Network Express. For more information, contact Jeff Fritz of the NIUF's Enterprise Network Data Interconnectivity Family at (304) 293-2060, or e-mail jfritz@wvnvm.wvnet.edu. *CA*

PAPER DETAILS EMF SHIELDING THEORY

In work supported by the Federal Aviation Administration, NIST researchers came up with a mathematical model and theory for predicting the electromagnetic-field shielding effectiveness of large metal enclosures with apertures and interior loading. The model also should allow for estimations of the average field strength inside enclosures such as electronic equipment cases and aircraft bodies. It can be used for any enclosure regardless of size, shape, type of material, and number of apertures, as well as for any frequency above a lower limit related to the dimensions of the enclosure. A report, *Aperture Excitation of Electrically Large, Lossy Cavities* (Technical Note 1361), is available from the National Technical Information Service. Call (703) 487-4650. *CA*

CdSSe LIGHT VALVE PRODUCES 600-IN. IMAGES

Using a solid-state tri-layer light valve, electronic CRT images can be amplified on screens up to 600 in. diagonal. Developed by LighTouch Systems Inc., Fremont, Calif., the light valve is designed with a patented cadmium sulfur selenide (CdSSe) technology. The high-carrier mobility of CdSSe has some advantages over competitive amorphous silicon and polysilicon technologies. The company claims that CdSSe offers higher performance, is easier and less expensive to produce, and requires no manufacturing toxins. The use of a large-area phototransistor tri-layer structure helps control light in a precise manner over a defined area. The optical amplifier has produced over 12-million-pixel images in the laboratory. Full-motion video can be switched at real-time rates. Applications for the technology include projection systems, medical imaging, and large format/high-resolution workstation displays. For more information, call LighTouch Systems at (510) 226-1700. *RN*

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Mini-Circuits 15542 ZFRSC-2050B
Mini-Circuits 15542 SPLITTER ZFSC-4-1W
Mini-Circuits 15542 SPLITTER ZFSC-3-1
RF/IF Designer's Handbook
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READER SERVICE 116

F134 Rev D

NEW TECHNOLOGY AT BIPOLAR CONFERENCE

A forum for technical communication focused specifically on bipolar and biCMOS technology is the basis for a conference scheduled for October 10 and 11 at the Marriott City Center Hotel, Minneapolis, Minn. Sponsored by the IEEE Electron Devices Society, in cooperation with the IEEE Circuits and Systems Society and the IEEE Twin Cities Section, the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) will consist of a two-day meeting with three parallel sessions. The conference includes a keynote speech on the future of bipolar in analog ICs, and discussions on low-power designs and the "curiosity or reality" of SiGe.

Also on tap are a series of papers on topics such as high-performance biCMOS and bipolar transistor technology and process integration. General-process integration issues will be presented. For technical or registration information, contact CCS Associates at (612) 349-4000 or fax (612) 349-9223. *CA*

POWERFUL RISC CPUS WAIT IN THE WINGS

Faster throughputs and multimedia support on-chip will highlight next-generation RISC microprocessors. That's the message expected to be heard at the upcoming Microprocessor Forum at the Hyatt Hotel, Burlingame, Calif., Oct. 18 and 19. The newest designs of the Digital Equipment Alpha processor, the Hewlett-Packard PA-8000 CPU, and the IBM/Motorola PowerPC microprocessor all will be unveiled. Also set for discussion are the latest 64-bit superscalar RISC CPUs from the MIPS Technology Div. of Silicon Graphics and Sun Microsystems Computer. In many of these processors, designers use architectural techniques such as superscalar instruction pipelines, as well as 64-bit data and 128-bit instruction paths. These techniques have been applied to supercomputers to achieve record-setting computational levels. Further details will be unveiled in the next issue of *Electronic Design*. *DB*

ANALYTIC SIMULATION IS FAST AND ACCURATE

ADM, a new circuit-simulation technology, uses an analytic technique to yield Spice-level accuracy with gate-level simulation performance. ADM was developed by Anagram Inc., Seattle, Wash., to provide timing simulation and power-analysis tools for submicron-IC design and verification. The ADM approach has major benefits over older technologies based on piece-wise-linear and RC simulation techniques. Speed and accuracy is achieved with analytic, closed-form output solutions for large-scale CMOS circuits. For digital circuits with up to 10,000 transistors, Anagram claims they provide 100 times speed up over Spice. In addition, the company says that accuracy is within 2% to 5% of digital timing simulation.

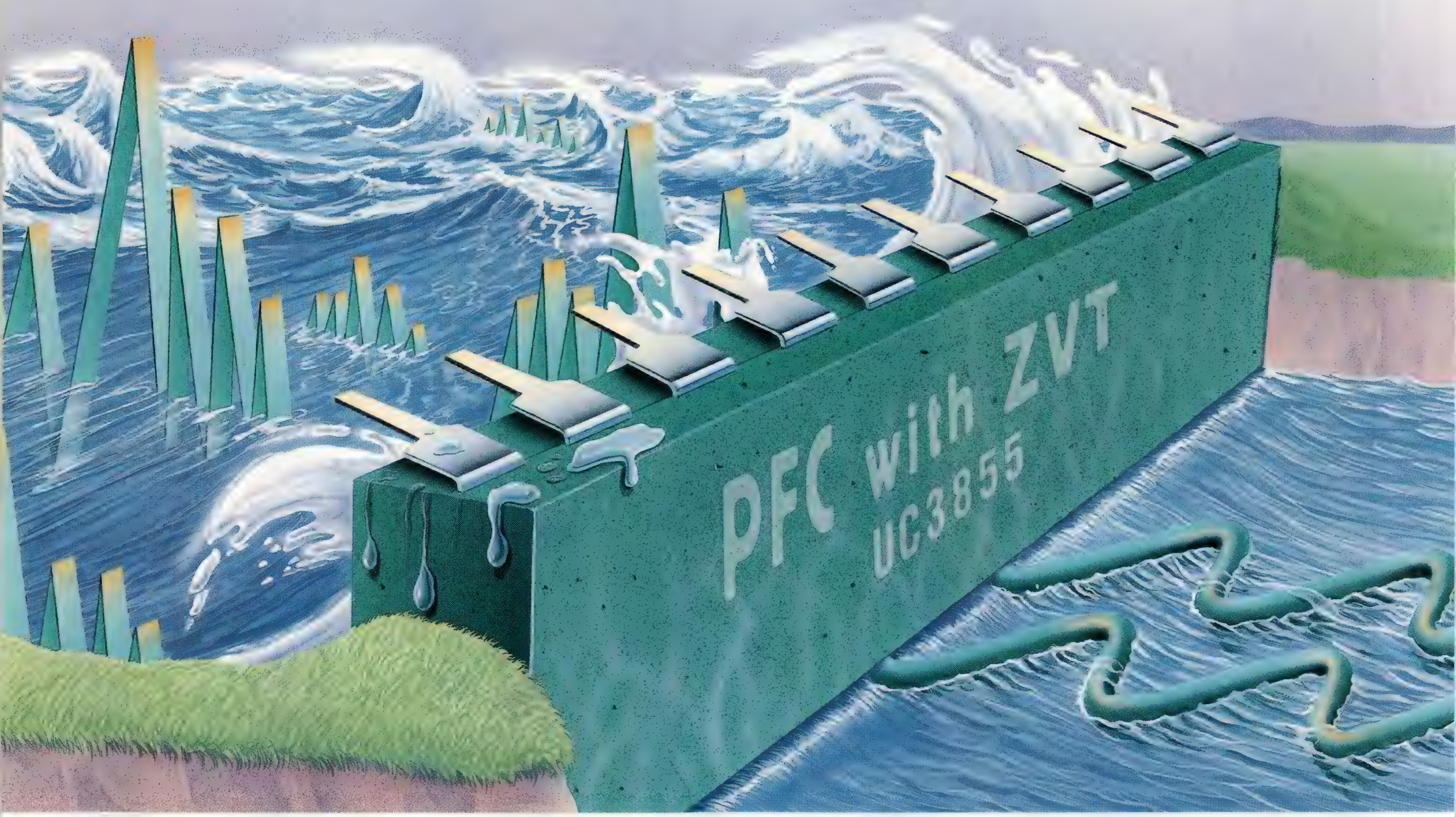
By treating all circuit nodes and branches uniformly, ADM can to simulate sophisticated circuit structures and non-digital behavior at the transistor level. Simulation times with the ADM proprietary algorithms scale almost linearly with the number of transistors. ADM performs simulation using existing model and process parameters, and therefore protects users' investments in transistor models. For more information on the ADM circuit-simulation technology, call Anagram at (206) 547-4417, or contact them by e-mail at sales@anagraminc.com. *LM*

UNIVERSITY LABS FOCUS ON EDA-TOOL RESEARCH

Cadence Design Systems Inc., San Jose, Calif., recently established the Cadence Berkeley Laboratories, Berkeley, Calif., to perform research and development in the area of electronic design automation (EDA). Applying breakthrough technologies, the labs will focus on applications that advance computer-aided-design (CAD) technologies.

By choosing a site in Berkeley, Cadence is encouraging a two-way exchange between its lab scientists and University of California at Berkeley researchers. The new organization has attracted specialists in the fields of logic synthesis, timing analysis and optimization, simulation, and formal verification. U.C. Berkeley professors Alberto Sangiovanni-Vincentelli and Robert Brayton have been instrumental in setting up the goals and research projects for the labs. In addition, Cadence Berkeley Labs is creating an opportunity for customers to participate in select research projects as Associate Scientists, which provides early access to technology developed in pilot projects. For more information about the labs, call Cadence at (408) 943-1234. *LM*

Control Rough Waves with Soft Switching



Reach new heights in power factor correction performance. The UC3855's unique "soft switching" technique dramatically reduces diode recovery and MOSFET turn-on losses. The result is super-high efficiency which enables higher frequency switching and more compact preregulator designs.

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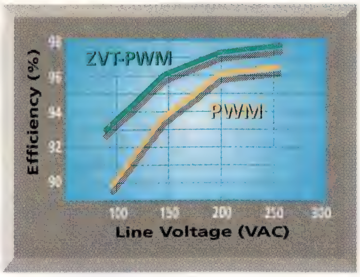

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READER SERVICE 156

Will your graphical programming language

bury

you under weeks of rewriting

your

existing test code, or let you leverage the

past

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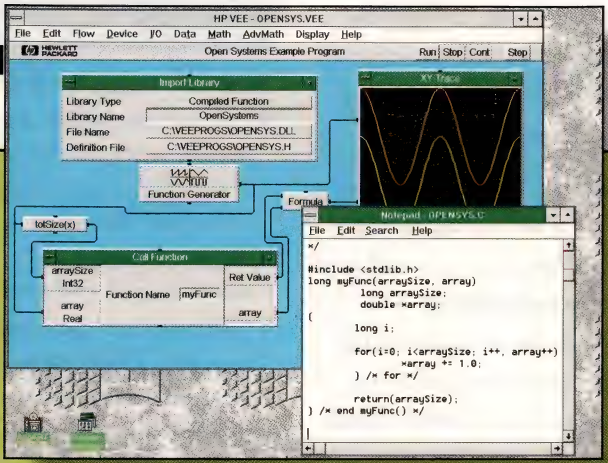


Library Type: Compiled Function
Library Name: OpenSystems
File Name: C:\VEEPROGS\OPENSYS.DLL
Definition File: C:\VEEPROGS\OPENSYS.H

arraySize Int32
array Real
Function Name: myFunc

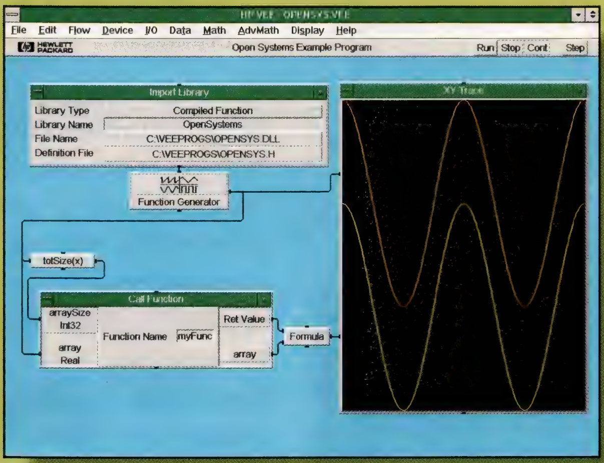
```
*/

#include <stdlib.h>
long myFunc(arraySize, array)
         long arraySize;
         double *array;
{
        long i;

        for(i=0; i<arraySize; i++, array++)
                *array += 1.0;
        } /* for */

        return(arraySize);
} /* end myFunc() */
```

You'll save a whole lot of hassle by choosing a graphical test programming language that can import your existing code, like the C routines above.



Library Type: Compiled Function
Library Name: OpenSystems
File Name: C:\VEEPROGS\OPENSYS.DLL
Definition File: C:\VEEPROGS\OPENSYS.H

arraySize Int32
array Real
Function Name: myFunc

Once you've brought in the code, HP VEE integrates it into your test program and displays the results.

Make the most of your time.

Tossing out all the text-based code you've written because you're about to switch to a graphical programming language is a tough decision. It's the test engineering equivalent to dumping your entire record collection when you buy a CD player.

In other words, it's costly.

It's also unnecessary. That is, if you use HP VEE, our visual engineering environment — the one graphical test development language designed by people who understand your need to leverage the past.

Make the most of your code.

Since HP VEE was designed with test engineering in mind, we knew you'd want standard ties (like DDE, DLL, named pipes, and shared libraries) to standard languages (including C, C++, HP BASIC, FORTRAN, Pascal, and Visual BASIC). So you won't waste time rewriting code.

More evidence that HP VEE is completely open is that it runs on any Windows-based PC, plus Sun, HP-UX workstations and embedded VXI controllers — making your test programs portable throughout your company.

Make the most of instrument control.

For complete instrument control we provide direct I/O, drivers, and driver writer tools that let you control every test instrument (and every instrument function) that'll ever see the inside of your lab...from any vendor.

So there it is. Several powerful reasons to use HP VEE. And one word of caution: If you bury your past, you may dig up some very nasty problems.

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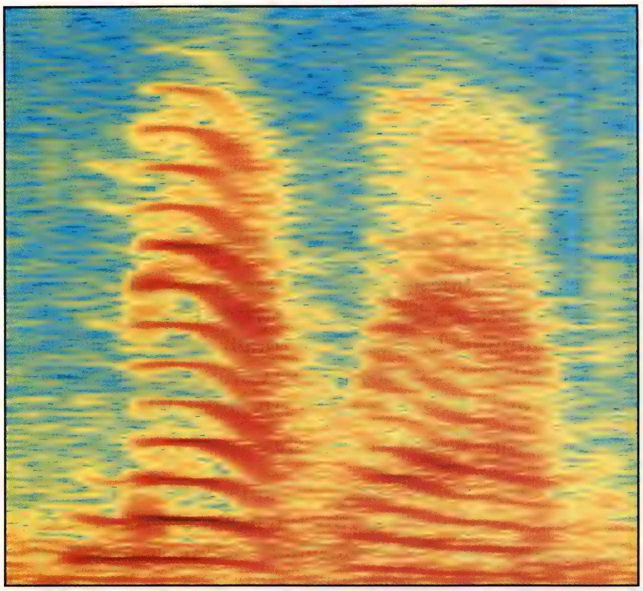
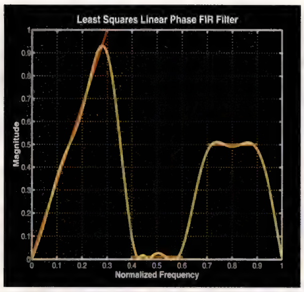


MATLAB simplifies analysis and algorithm development with integrated modeling, design and graphical tools. This spectrogram shows how a speech signal varies with time and frequency.

Speak the language of signal processing with MATLAB®

The MATLAB Signal Processing Toolbox is a powerful interactive environment for signal analysis, algorithm development, and DSP design.



Leading-edge filter design tools make it easy to design filters to fit any specification.

Because its matrix language is ideal for vector processing and data analysis, MATLAB helps you solve the widest range of signal processing problems.

Signal processing power

The Signal Processing Toolbox gives you an unrivaled ability to filter, model, and analyze signals and time-series data. Powerful functions let you perform FFTs, spectral estimation, and filter design in a single step, and display the results automatically.

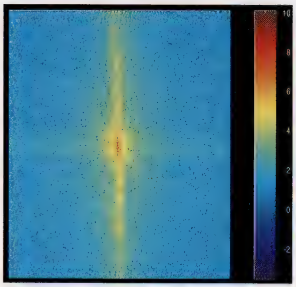
Without writing a single line of C or Fortran, you can easily explore, create, and apply the innovative signal processing tools that let you keep up with—and advance—the leading edge.

Rapid algorithm development

You create DSP algorithms in MATLAB just as you would write them mathematically. As a result, you can rapidly validate your designs long before you commit to a full implementation.

Your work always draws upon world-class tools, whether you rely on classical methods or invent state-of-the art technology.

MATLAB brings a foundation of over 500 math, scientific, and engineering functions to your desktop. Each function is tuned for maximum efficiency and numeric reliability. So you always get immediate, accurate results.



Visualization of a 2-D FFT. Efficient FFT algorithms form the basis for powerful spectral analysis and estimation functions.

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Picture the Power

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UPCOMING MEETINGS

OCTOBER

1994 IEEE Bipolar/BICMOS Circuits & Technology Meeting, Oct. 10-11. Marriott City Center Hotel, Minneapolis, MN. Contact Janice Jopke, 6611 Countryside Dr., Eden Prairie, MN 55346; (612) 934-5082; fax (612) 934-6741.

1994 International Workshop on Active-Matrix LCDs, Oct. 10-11. Hyatt Regency Hotel, Monterey, CA. Contact Miltiadis K. Hatalis, 19 Memorial Dr. West, Lehigh University, Bethlehem, PA 18015; (215) 758-3944; fax (215) 758-4561.

1994 IEEE International Conference on Computer Design: VLSI in Computers & Processors (ICCD), Oct. 10-12. Royal Sonesta Hotel, Cambridge, MA. Contact IEEE Computer Society, Volunteer Services Dept., 1730 Massachusetts Ave. N.W., Washington D.C. 20036-1903; (202) 371-1013.

1994 Symposium on Low-Power Electronics, Oct. 10-12. The Doubletree Hotel at Horton Place, San Diego, CA. Contact Diane Suiters, 655 15th St. NW, Suite 300, Washington, DC 20005; (202) 639-4255; fax (202) 347-6109.

1994 International Display Research Conference, Oct. 10-13. Hyatt Regency Hotel, Monterey, CA. Contact Ralph Nadell, Palisades Institute for Research Services Inc., 201 Varick St., New York, NY 10014; (212) 620-3341.

1994 1st European Workshop on Mobile/Personal SATCOMS, Oct. 11-12. ESA/ESRIN, Rome, Italy. Contact Francesco Vatalaro, Dipartimento Di Ingegneria, Elettronica, Universita Di Roma Tor Vergata, Via della Riccerca Scientifica 00133 Rome, Italy; (39)-6-72594464; fax (39)-6-72594454.

1994 3rd International Conference on Intelligence in Networks (ICIN '94), Oct. 11-13. Bordeaux-Palais des Congres, Bordeaux, France. Contact Jean Rivenc, ADERA, BP 196, 33608 Pessac Cedex, France; (33)-56-15-11-56; fax (33)-56-15-11-60.

It seems like **half** your life is spent developing test programs. But then, that's **the cost** of using the wrong programming language.

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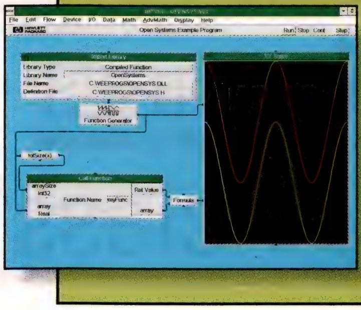

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UPCOMING MEETINGS

OCTOBER

NORTHCON '94, Oct. 11-13. Washington State Convention Center, Seattle, WA. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (310) 215-3976; fax (310) 641-5117.

15th Aerospace Testing Seminar, Oct. 11-13. Radisson Plaza, Los Angeles, CA. Contact J. Kendrick, Institute of Environmental Sciences, 940 E. Northwest Hwy., Mount Prospect, IL 60056; (708) 255-1561.

1st International Conference on Flex Circuits, Oct. 12-14. Sunnyvale Hilton, Sunnyvale, CA. Contact Subash Khadpe at (610) 799-0419.

Singapore Informatics '94, Oct. 13-16. Singapore World Trade Center, Singapore. Contact Ellen Wong, Commerce Tours International Inc., 870 Market St., Suite 920, San Francisco, CA 94102; (415) 433-3072; fax (415) 433-2820.

1994 GaAs RED Workshop, Oct. 16. Wyndam Franklin Hotel, Philadelphia, PA. Contact William J. Roesch, TriQuint Semiconductor, (503) 644-3535, ext. 273.

1994 Wireless Circuits, Interconnection, and Assembly Workshop, Oct. 16-19. Paradise Valley, AZ. Contact Sharon Aspden, conference coordinator, Rogers Corp., 100 S. Roosevelt Ave., Chandler, AZ 85226; (602) 961-1382; fax (602) 961-4533.

1994 IEEE GaAs IC Symposium, Oct. 16-19. Wyndham Franklin Plaza Hotel, Philadelphia, PA. Contact Donald C. D'Avanzo, Hewlett-Packard Co., 1412 Fountaingrove Pkwy., Santa Rosa, CA 95403; (707) 577-2644.

1994 1st International Conference on Materials for Microelectronics, Oct. 17-19. Hotel Feria Palace, Barcelona, Spain. Contact Juliet A. Upton, The Institute of Materials, Conference Dept., 1 Carlton House Terrace, London SW1Y 50B, United Kingdom; (44)-71-235-1391; fax (44)-71-823-1632.

1994 International Conference on Neural Information Processing (ICONIP '94), Oct. 17-20. The Swiss Grand Hotel, Seoul, Korea. Contact ICONIP '94. Seoul Secretariat, c/o INTERCOM Convention Services Inc., SL Kang Nam, P. O. Box 641, Seoul 135-606, Korea; (82)-2-515-1560; fax (82)-2-516-4807; e-mail: ICONIP@cain.kaist.ac.kr.

5th International Conference on Signal Processing Applications & Technology, featuring DSP World Expo, Oct. 18-21. INFOMART Conference and Exhibition Center, Dallas, TX. Contact Cynthia Margulis, DSP Associates, 49 River St., Waltham, MA 02154; (617) 891-6000.

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READER SERVICE 102

IC'S PC-BOARD CAPACITORS CARRY 50-MBAUD LOGIC ACROSS 2400-V ISOLATION BARRIER

Often, it becomes necessary to carry one or more serial digital pulse trains in one or both directions across a high-voltage isolation barrier. The link between a microcontroller and the control system for a multi-horsepower motor represents a good example of this type of application, a job that's generally handled by optocouplers.

However, optocouplers draw large current pulses from the power-supply rails to drive their LEDs, particularly in high-speed applications. These current pulses, in turn, put noise spikes on the power-supply rails. In addition, to handle the aging problems endemic to optocouplers (output light from the LEDs decreases with use), the current pulses are initially greater than required for normal operation.

To alleviate this problem, designers at Burr-Brown came up with a unique coupling architecture and technique employing a pair of biCMOS ICs and capacitors formed by pc-board traces. The capacitors carry the pulse train across the barrier.

The first application of the technique resulted in a dual bidirectional digital coupler called the ISO150 *(Fig. 1)*. The device transmits two dc-to-50-Mbaud CMOS/TTL pulse trains between two points whose potential difference can be up to 2400 V rms. That is, it transmits the signal across a 2400-V isolation barrier. Each coupler channel needs just 25 mW of power. In addition, unlike optocouplers, the ISO150's performance doesn't change with time.

Each dual coupler IC consists of four independent transceivers: 1A, 1B, 2A, and 2B. Every transceiver has its own Data pin (D_{1A}, D_{1B}, D_{2A}, and D_{2B}) and Mode-Select pin ($R/\overline{T}_{1A}$, $R/\overline{T}_{1B}$, $R/\overline{T}_{2A}$, and $R/\overline{T}_{2B}$).

Observing one channel's operation basically illustrates how the coupler works *(Fig. 2)*. The transceiver on side A of the isolation barrier is in the transmit mode ($R/\overline{T}$ is low), while the transceiver on side B is in the receive mode ($R/\overline{T}$ is high). The TTL or CMOS input comes in on the Data (Dx) pin of side A, the input to a CMOS gate. The circuit trips when the input voltage reaches 1.5 V and 450 mV of hysteresis is provided. To ensure that high-frequency noise doesn't create any false signals, a "glitch filter" eliminates all input pulses nominally less than 8 ns wide as long as valid input pulses offer rise times of less than 200 ns.

Pulses from the transmitter section of each transceiver drive the barrier capacitors with a balanced (differential), complementary waveform at data rates from dc to 80 Mbaud. They create a loop current that flows through the receiver's current-sensing input stage. A transceiver will operate like an optocoupler when in the transmit mode, taking its power from the signal and sending it across the barrier without connecting a power supply to the transmitter side of the barrier.

The receiver section of the transceiver is put into the receive mode and its input senses the current pulses. The input stage, an analog circuit, rejects common-mode voltages while amplifying differential voltages. After amplification, the input signal is latched in the output flip-flop, which remains latched until a complementary signal arrives from the transmit side of the barrier. When the receive mode is selected, the output impedance of the nMOS and pMOS drivers are matched to minimize pulse-width distortion when driving capacitive loads.

The capacitors, which carry the signals across the isolation barrier, employ the parasitic capacitance between traces on a tiny pc board encapsulated within the IC's plastic package *(Fig. 3)*. Most pc-board designers try to avoid situating pc-board traces close together because of the undesired capacitance—particularly if the traces are carrying fast pulses. However, Burr-Brown deliberately created close parallel traces to form the four 0.4-pF capacitors that carry signals across the isolation barrier.

In earlier linear isolation-amplifier designs, the company's designers used capacitors formed by portions of the leadframe. They rejected that technique, though, for the ISO150's capacitors. It was their first two-channel isolator and they were unable to design a leadframe topology that

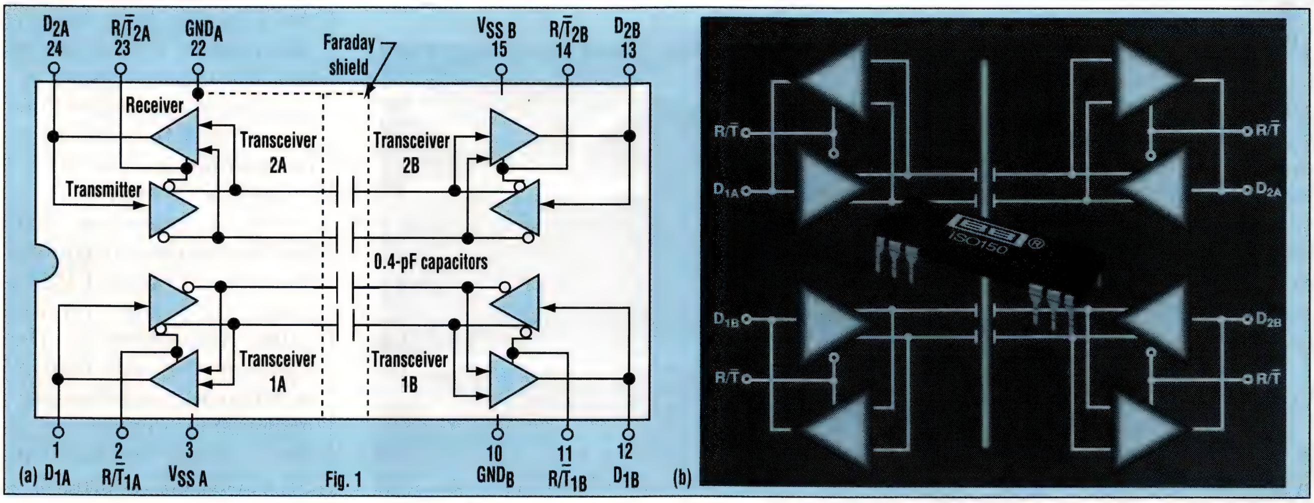


Fig. 1

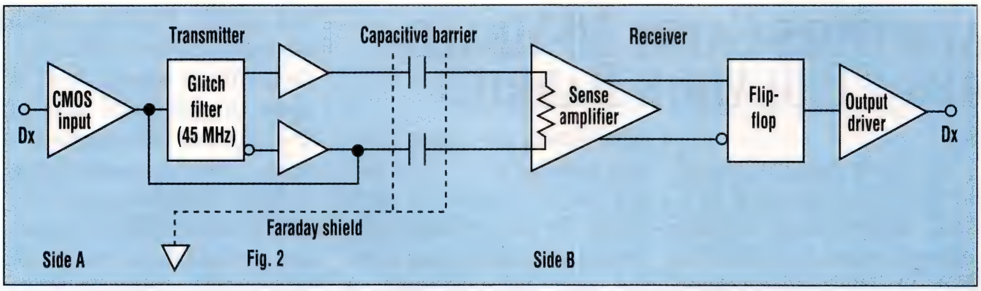


Fig. 2

would create the required four capacitors while avoiding the detrimental effects of unintended parasitic capacitance between channels.

The designers also knew that the leadframe technique was sensitive to electrostatic fields, which could cause false switching if the isolator was exposed to a dynamic, high-voltage field (instead, the pc board adds a Faraday shield around the capacitors to minimize the effects of such stray fields, see Fig. 2). Finally, even if the leadframe could be used to form the capacitors, it would have taken up too much real estate in the package.

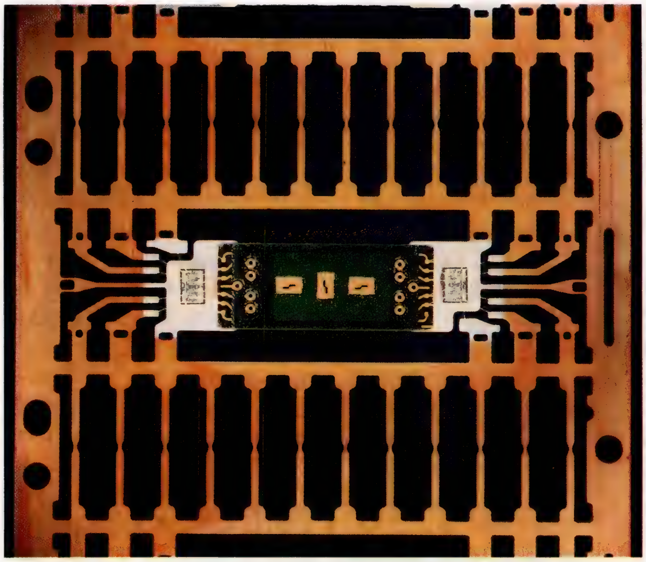
As an alternative to the leadframe technique, the basic construction of the ISO150 consists of a pair of biCMOS chips, the four capacitors built into the pc board, and a custom leadframe for the 24-pin package (pins 4 through 9 and 16 through 21 are missing). On the pin-1 end of the package, the leadframe supports one of the chips.

As noted earlier, both channels of this dual-channel die can be configured to either transmit the signal across the barrier by driving two capacitors, or receive the signal from two capacitors and convert it into a digital output. The leadframe also supports one side of the pc board. Bond wires are connected from the chip to the pins as well as from the chip to one side of the capacitors. On the pin-13 end of the isolation barrier, the leadframe supports the other end of the pc board and the second dual transceiver chip. The pc board, not the leadframe, spans the barrier.

The ISO150 also is available in an SOIC. To maintain the creep distance required to handle the potential of 2400 V rms and find space for the four capacitors in this package, the IC required a 28-pin SOIC package. However, like the DIP, the SOIC package still has only 12 pins, six at each end.

For additional information, call Burr-Brown's Stephan Baier at (800) 548-6132.

FRANK GOODENOUGH

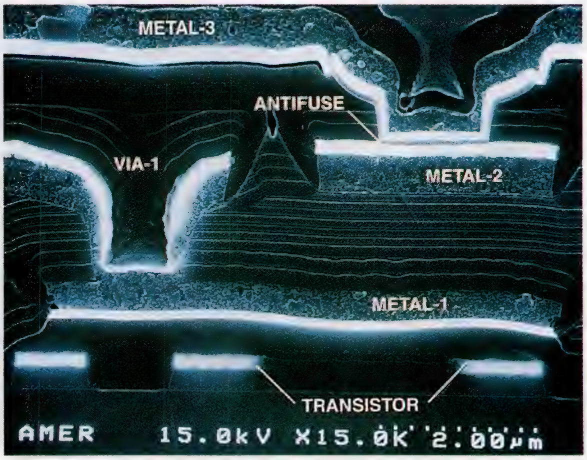


MERGER OF TRIPLE-LEVEL METAL AND ANTIFUSES YIELDS HIGH-DENSITY FPGAS

The attractiveness of using one-time-programmable antifuses in field-programmable logic centers on their small size, which makes it possible to integrate fine-grain high-density programmable logic into silicon. But today's schemes still occupy area between cells, even if they're above the silicon, forcing chip area to expand to accommodate the antifuses.

By placing the antifuses above the silicon and between two of the metal interconnection layers in a three-level-metal process, designers at Xilinx Inc., San Jose, Calif., think they've licked this problem. As a result, they believe this scheme solves one of the key density issues toward achieving usable densities of 6000 to 40,000 gates on moderately-sized chips.

Xilinx's MicroVia technology occupies less than half the chip area of equivalent SRAM-based FPGAs using the same process rules. Consequently, the company can sell equivalent-density, one-time-programmable devices at a much lower price than SRAM-based reprogram-

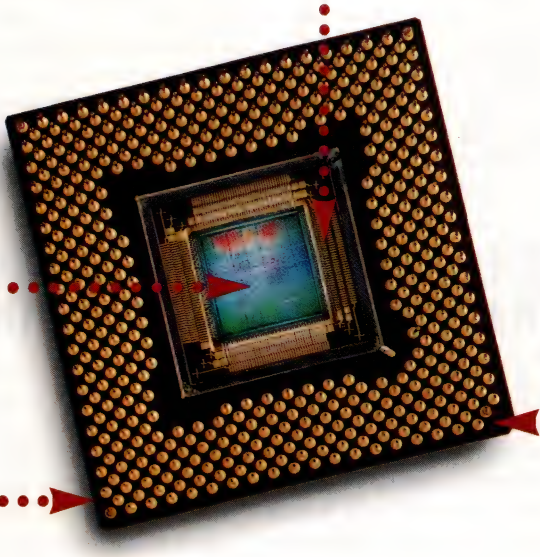


BIG DIE

0.560 inches square, embedded memory, and over 100,000 gates. A **very** big die.

BIG I/O

504 I/O pads, arranged in two rows around the periphery of the chip.



BIG HEAT

Running at 20 MHz and generating eight watts of power. With this much power, we had to pipeline the heat away from the die.

BIG PACKAGE

The only off-the-shelf package that met all the technical specifications was three to four times too expensive. The solution: a custom ceramic PGA, shown here at actual size.

NO BIG DEAL

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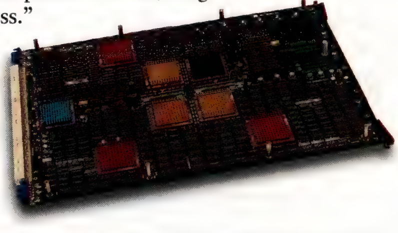

That's what IKOS Systems found out recently, when they brought the custom gate array you see above to American Microsystems, Inc. To create their next-generation hardware accelerator for logic simulation, IKOS needed to embody their evaluation algorithms in four ASIC designs with over 300,000 gates of custom logic in all.

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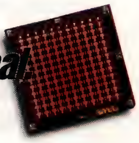

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mable chips, or offer much higher density devices.

Combining three levels of metal interconnections and the metal-to-metal antifuses between the second and third metal layers allows much denser logic to be integrated, simply because the logic elements can be packed closer together. The denser logic also enables users to implement much more complex logic functions. In addition, since the fuses are directly underneath the metal lines, they don't occupy the wiring channels, giving chip designers more routing resources. That, in turn, allows the place-and-route software tools to achieve 100% utilization.

The novel technology is based on an amorphous silicon metal-to-metal shorting scheme (an antifuse). This method somewhat resembles the scheme employed by Quicklogic Corp., Santa Clara, Calif., but is radically different from the polydiffusion/oxide-nitride-oxide scheme adopted by Actel Corp., Sunnyvale, Calif. To make the logic chips, the MicroVia manufacturing process requires just two additional mask steps that supplement the basic CMOS process used to fabricate the logic. The change in processing involves the deposition of the programmable amorphous-silicon layer inside the via holes between the level-2 and level-3 metal layers *(see the photo)*.

In its unprogrammed state, the amorphous silicon layer acts as an insulator. As a result, it keeps the metal layers disconnected. With the proper biasing (programming), however, a low-resistance filament forms in the amorphous silicon layer. That filament connects the two metal layers, forming a signal path. Key to the process is precise thickness control of the antifuse layer to ensure a consistent programming-voltage level across the chip.

Designers at Xilinx are preparing a family of antifuse-based FPGAs based on a sea-of-gates architecture (its expected release is scheduled for the first half of next year). Such an architecture will make the FPGAs appear much more like a gate-array replacement than current-generation FPGAs. Internally, the company has already fabricated a 6000-gate chip as a proof of concept. It plans to provide a detailed view of the technology at the IEEE International Electron Devices Meeting in Washington D.C., Dec. 11-14.

For further information, contact Xilinx's Lee Farrell at (408) 559-7778.

DAVE BURSKY

ECL CIRCUITS SHOW RENEWED PROMISE THANKS TO ACTIVE PULL-DOWN DESIGNS

In the arena of high-performance systems, one of the many difficult problems designers face is achieving lower power-dissipation levels and faster circuit delays for CMOS or conventional ECL circuits. But, recent improvements circumvent ongoing problems associated with the ECL circuit, pumping new life into the device.

There are two inherent advantages to using ECL structures over other conventional circuits. Primarily, the switching current in a bipolar differential pair is much faster than what can be achieved with MOS transistors. On top of that, however, the voltage swing of a signal propagated through a wire is much smaller than that of a comparable CMOS structure.

The one main disadvantage to using ECL driver circuits is they dissipate large amounts of power. Recent attempts to remedy this age-old problem and speed up circuit performance has resulted in the proposal of various types of active pull-down (APD) ECL circuits to replace traditional resistor or current-sourced emitter-follower circuits.

For example, the ac-coupled APD ECL circuit can operate at a higher speed with smaller power dissipation than conventional ECL circuits. When the output goes from a high level to a low level, the capacitors are able to improve the fall time of the load capacitance voltage by enhancing the pull-down current. When the output goes from low to high, pull-down current is suppressed.

The APD ECL circuit, while offering improvements over conventional ECL driver circuits, still has several drawbacks. It requires adding more elements, such as a capacitor, and its performance degrades due to fluctuations of power-supply voltage and temperature. Furthermore, other proposed devices have burdensome restrictions, such as requiring high-performance pnp devices, special-capacitor structures, loss of wired-OR capability, and use of both true and complement gate outputs.

The issue of improved capabilities for ECL driver circuits as well as other vital issues will be discussed by many researchers from a variety of academic and commercial institutions. These researchers will meet at the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), scheduled to take place Oct. 10-12 at the Marriott City Center Hotel, Minneapolis, Minn.

In one session on ECL circuitry, authors will specifically address the development of new APD-ECL driver circuits to meet the changing needs of designers. One circuit configuration, an APD-ECL circuit with full compensation for fluctuations of voltage and temperature, comes from researchers at the System LSI Laboratory of Mitsubishi Electric Corp., Hyogo, Japan. This circuit

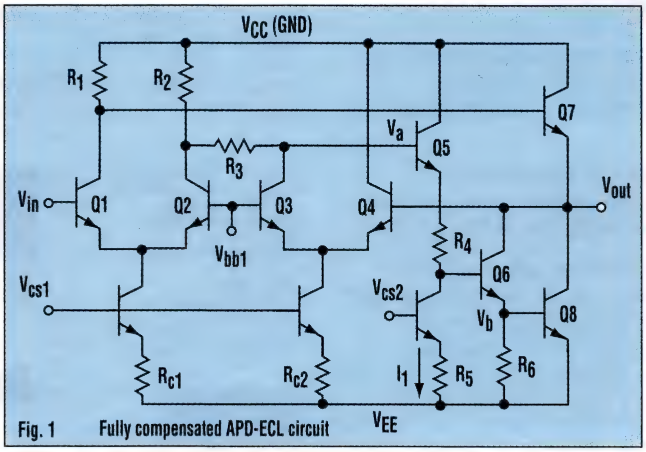
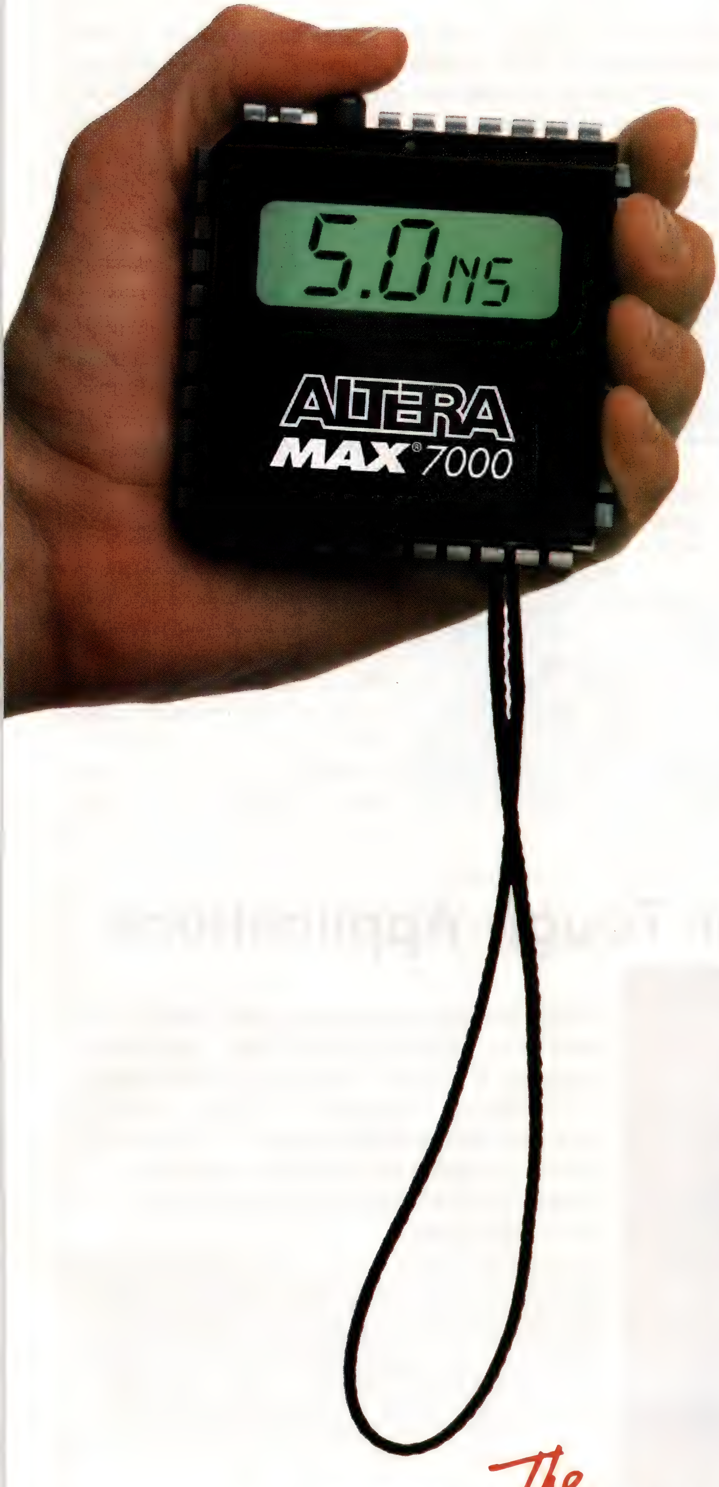


Fig. 1 Fully compensated APD-ECL circuit



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adjusts its pull-down capability according to its load capacitance, using a feedback circuit rather than capacitors *(Fig. 1)*.

According to the authors, "In this circuit, the driving capability for a pull-down transition adapts to the change in the level output voltage. When the load capacitance is larger, the turn-on of the bipolar resistor Q8 takes a longer period. In this sense, the circuit adjusts its driving capability according to its load capacitance". In addition, the current flowing through bipolar transistor Q8 is compensated against any temperature or power-supply-voltage (V_{EE}) fluctuations.

Spice simulations of the Mitsubishi APD-ECL circuit, under the set conditions of a power dissipation of 2.5 mW with a load capacitance of 0.8 pF, show that it's 50% faster than a conventional ECL circuit. Also, at an operating frequency of 600 MHz and a load capacitance of 0.8 pF, the circuit's power dissipation is 47% lower than a comparable CMOS circuit and 29% lower than the conventional ECL circuit.

Another ECL circuit is described by Vojin G. Oklobdzija from the Department of Electrical and Computer Engineering at the University of California at Davis *(Fig. 2)*. The ECL gate exhibits an improved speed-power product over other conventional circuits, in part due to the combination of a push-pull output stage driven by a controlled current source. The circuit has improved driving capabilities and speed, and uses an order of magnitude less power than a regular ECL gate. Full bipolar realization of this circuit also is possible.

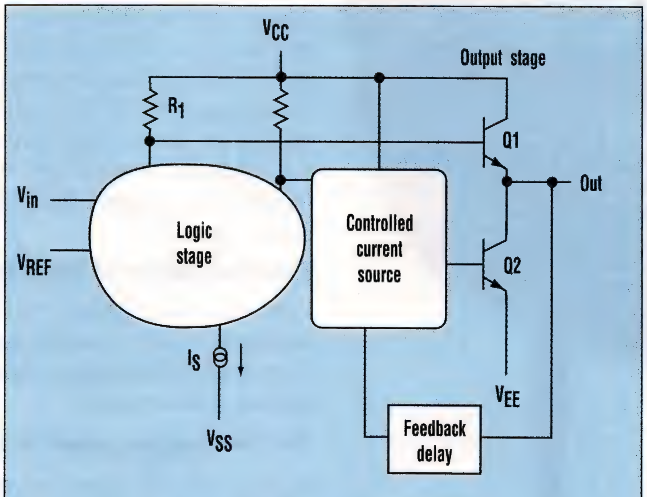

Fig. 2

FCCS APD-ECL circuit

The new circuit, FCCS-APD-ECL, utilizes a feedback-controlled current source in an active-pull-down ECL configuration. The controlled current source is used to inject current into the pull-down transistor of its output stage during transition pe-

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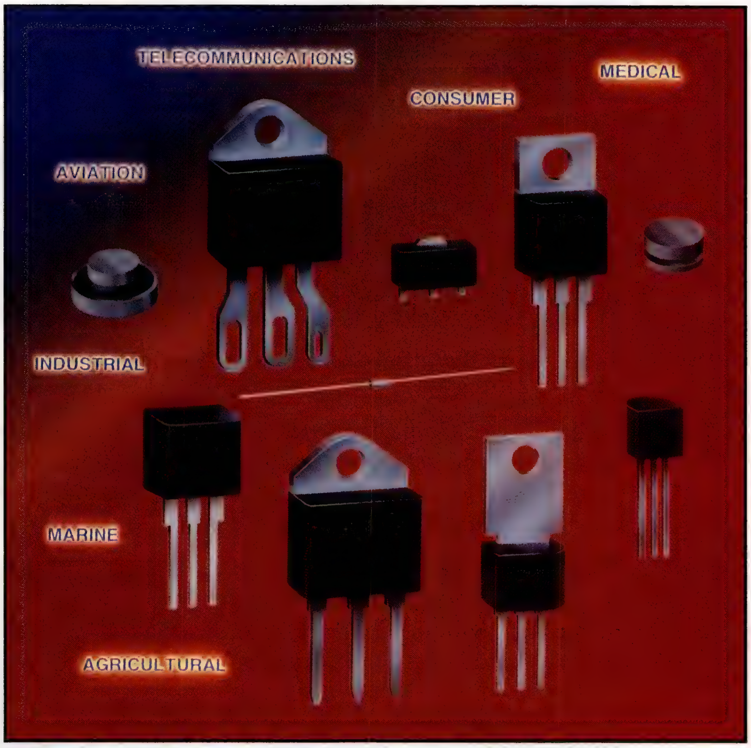

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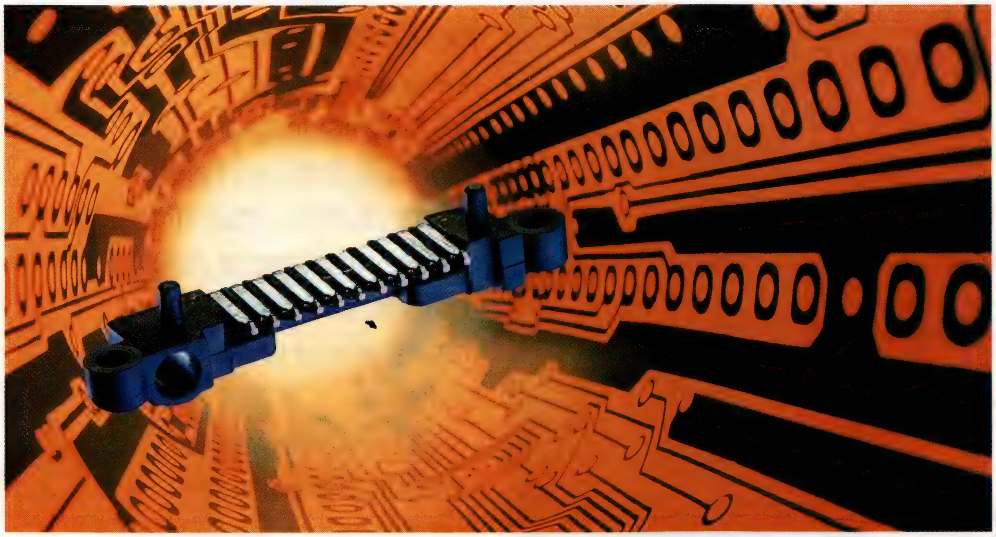

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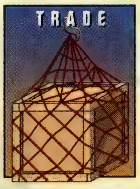

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riods. While in a steady state, this current is reduced to its minimum value. By carefully tuning the signal levels and their timing relationship, increased dynamic and reduced static current in the output stage can be achieved. Thus, the major part of the power budget is consumed in the logic stage rather than the output stage.

Additional circuit benefits include a decoupling of the logic stage from the noise usually generated in the output stage; overall power reduction; and the ability to cascode the logic in more than one level. Thanks to the cascoding feature, more complex operations are also possible within a single ECL tree.

The circuit's one main disadvantage is that it can't handle wired-OR functions. This is offset, though, by its simple structure and its ability to handle higher-capacitance loads.

For more information on APD-ECL driver circuits, or general BCTM conference details/registration, contact the 24-hour voice-mail conference information center at (612) 934-5082, or fax at (612) 934-6741.

CHERYL AJLUNI

SELF-LEARNING NEURAL CHIPS PROMISE NEURAL-NETWORK APPLICATIONS

Recent developments in the hardware implementation of neural networks have shown promise for applications in many fields, including image recognition, real-time control, and signal processing. A new approach to building and training these networks may be a significant step toward the practical application of this technology.

Novel, nonlinear silicon neural-network elements have been successfully prototyped by professor Fathi Salam of the Michigan State University Electrical Engineering Department in Ann Arbor. The tiny, modular chips were the topic of Salam's presentation at the IEEE World Congress on Computational Intelligence, held in Orlando, Florida, June 26 to July 2. The chips feature a modular architecture implemented in analog CMOS with feedforward tuning and on-chip learning capability.

Until a few years ago, neural networks weren't implemented in hardware, but rather simulated by complex, slow-executing software on computers. Before physical circuits arrived, these simulated neural networks were usually limited to non-real-time applications such as financial analysis.

Now that some of the first neural-network silicon chips are being fabricated, one of the more interesting challenges in creating larger networks involves

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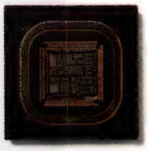

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the enormous task of training the network to produce reliable results.

One significant advance in this area is a technique called on-chip learning. Here, circuitry is added to the chip that compares the output of a network element against the *desired* output and adjusts the weight or path conductivity of the neural connections automatically. In the implementation of artificial neural networks, hardware on-chip learning capability has been in demand while software-based learning has become a time-consuming effort.

Without on-chip tuning, the results must be compared externally, and new weights calculated and finally adjusted from the outside. In many applications, hardware on-chip learning is superior, providing critically fast weight-convergence (on the order of microseconds to milliseconds) as well as real-time processing (on the order of microseconds).

With the limited size of the networks that can be housed in a single chip, an expandable, modular design becomes necessary for large-scale neural-network applications. The two prototype elements that were initially fabricated were configured with two outputs and either four or six input nodes.

The tiny, modular chips can be connected vertically in any order to increase the number of neurons in any layer or connected horizontally to boost the number of layers. By creating these horizontal and vertical matrices, the chips can be cascaded to achieve a large network.

Test results demonstrate the successful operation of the chips with on-chip learning in real-time experiments. Demonstration applications of the chips in three examples of adaptive signal processing, filtering, and prediction were presented at the World Congress. In addition, a three-chip neural-network structure with four inputs, two outputs, and a four-layer hidden structure was tested successfully.

Once the self-learning features trained the array to recognize the relationships between data-series histories, the resulting neural network could predict future time series within microseconds. While this capability is of great relevance to image-processing and compression applications, it will most likely find many other uses as the technology evolves.

Other applications envisioned for this new technology may include aircraft control systems as well as industrial process control. The quick response time and rapid learning capability of this architecture may also have military uses.

For further information, contact Professor Fathi M.A. Salam at the Systems, Circuits, and Artificial Neural Networks (SCANN) Laboratory, Department of Electrical Engineering, Michigan State University, East Lansing, MI 48824; (517) 355-5066.

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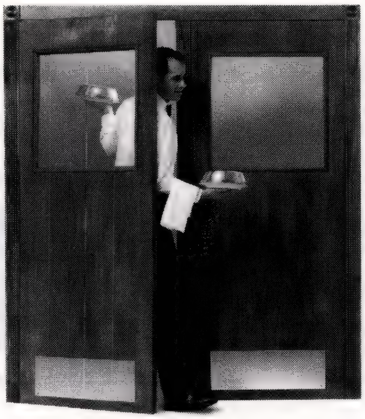

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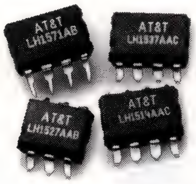

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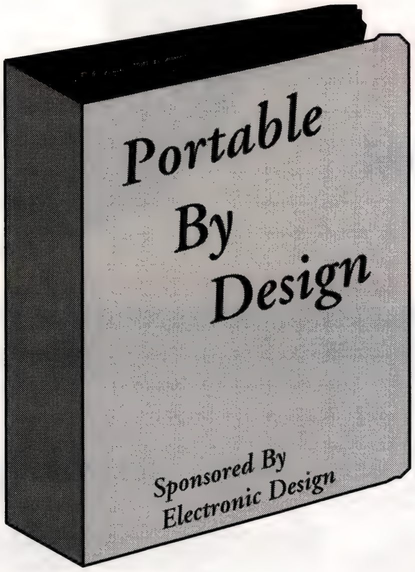

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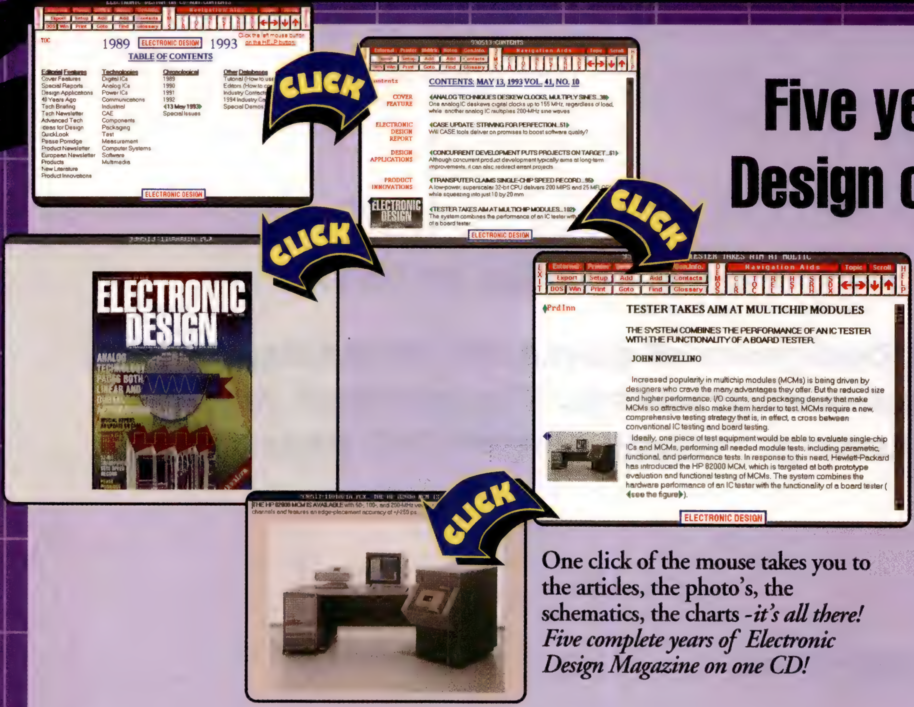

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PrdInn

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure).

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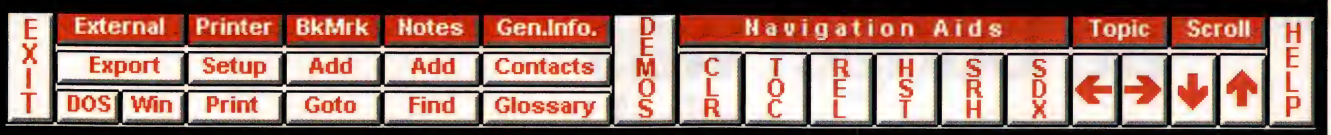

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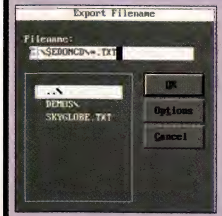

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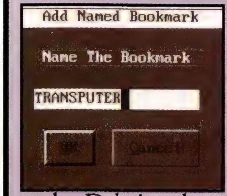

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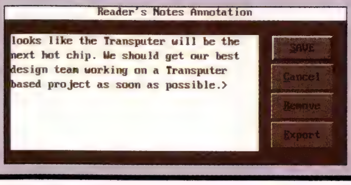

looks like the Transputer will be the
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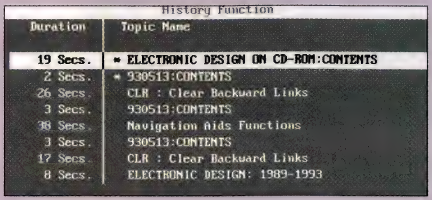

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                History Function
 Duration    Topic Name

 19 Secs.  * ELECTRONIC DESIGN ON CD-ROM:CONTENTS
  2 Secs.  * 930513:CONTENTS
 26 Secs.    CLR : Clear Backward Links
  3 Secs.    930513:CONTENTS
 38 Secs.    Navigation Aids Functions
  3 Secs.    930513:CONTENTS
 17 Secs.    CLR : Clear Backward Links
  8 Secs.    ELECTRONIC DESIGN: 1989-1993
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REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

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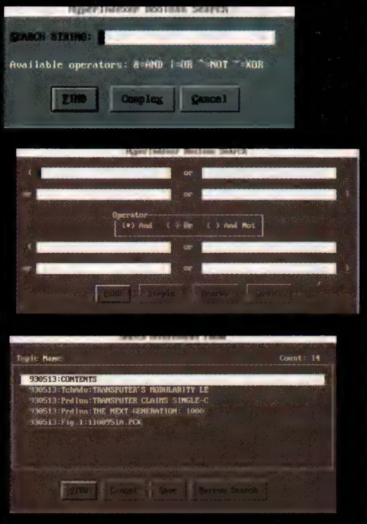

SEARCH STRING:
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Topic Name Count: 14

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930513:CONTENTS
930513:TchAdv:TRANSPUTER'S MODULARITY LE
930513:PrdInn:TRANSPUTER CLAIMS SINGLE-C
930513:PrdInn:THE NEXT GENERATION: 1000
930513:Fig.1:1100951A.PCX
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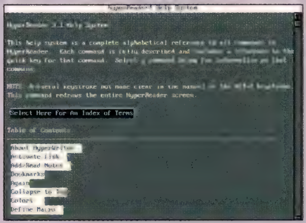

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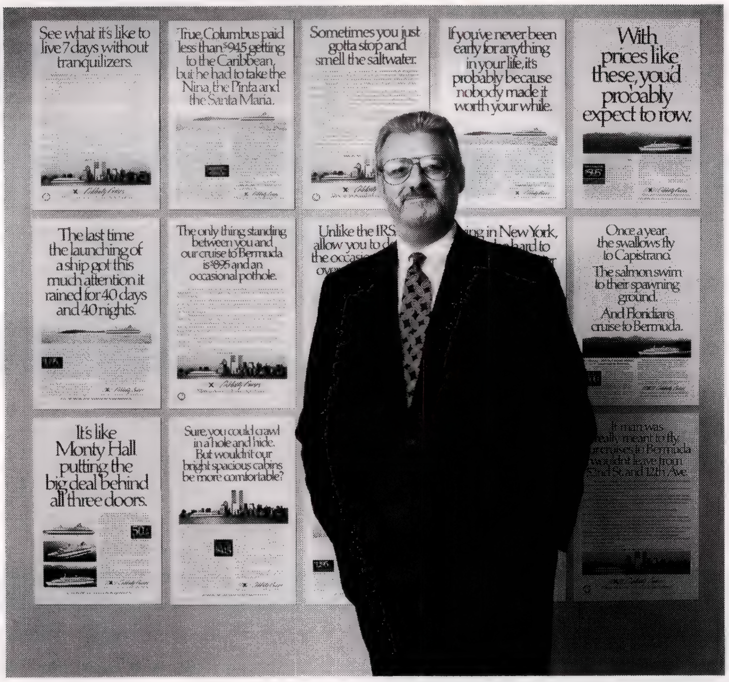

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True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
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If you've never been early for anything in your life, it's probably because nobody made it worth your while.
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The only thing standing between you and our cruise to Bermuda is $895 and an occasional pothole.
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It's like Monty Hall putting the big deal behind all three doors.
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Photo: Frank Moscati

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

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MULTIFUNCTION CARDS POSE DESIGN CHALLENGES

GENERATING A SECOND INTERRUPT AND ELIMINATING NOISE ON PCMCIA CARDS REPRESENT MAJOR ENGINEERING OBSTACLES.

RICHARD NASS

Here's a scenario that seems to be getting all the more common: You're at your desk working on a subnotebook computer, in the process of downloading a very large file. The boss comes in and wants to discuss a file that's on the local-area network. Because there's only one PCMCIA slot in the computer, and you've got the modem card plugged in (and not the LAN card), what do you do?

This problem exists because PCMCIA card developers have been unable to put more than one function on a card. While multifunction add-in boards exist for desktop PCs, that's not the case for PCMCIA cards. The main reason for a lack of multifunction PCMCIA cards is a flaw in the specification—there's only one interrupt available. The PCMCIA Committee realizes the problem exists, and is in the process of standardizing a technique that would permit multifunctionality. But until that time, card designers are navigating through uncharted waters.

Designers now are developing ways to generate a second interrupt. One such approach is embodied in a card released last February, the CreditCard Ethernet+Modem developed by Xircom Inc., Calabasas, Calif. But Xircom also has had difficulties solving the interrupt problem. In fact, some users report that the card doesn't perform the multifunctionality correctly.

Several design rules must be adhered to when building a multifunction PCMCIA card. For example, it's important to tie all function-specific information to the configuration information within the Card Information Structure (CIS). In addition, a designer must allow for independent use of each function on the card by including the ability to individually enable, control, disable, and report the status for each function. Another design criteria is the support for existing software that may be unaware of a card's interrupt-sharing ability. By eliminating changes to socket hardware, the impact on existing hardware and software will be minimized.

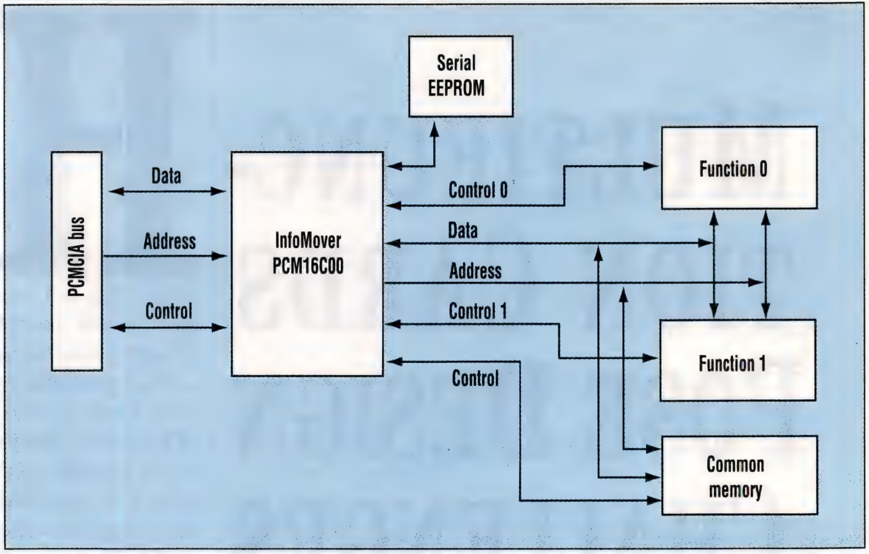
Some reserved pins on the PCMCIA connector could potentially be utilized for the second (or more) interrupt signal(s). To use these pins, however, the host-computer controller would have to be redesigned. This would remove the backward compatibility with existing cards.

HOW TO INTERRUPT

There are many different ways to perform multiple functions on one card, some of which work better than others. The first is a multimode approach that employs a serial interface. In this scheme, the same I/O port is employed to communicate with the host-computer system. However, it's used differently at different times, depending on which function requires use of the port.

The second approach is one that's proprietary for each manufacturer. It requires a special host-computer driver that can determine which function on the card is actually requesting attention.

Another proprietary technique uses a signal called "status change" to generate a second interrupt. This can



1. THE INFOMOVER PCM16C00 **designed by National Semiconductor Corp. conforms to the proposed multifunction standard. It shares the interrupt line using either a pulse or level mode. A PCMCIA interrupt request is asserted whenever the interrupt signal from either function on the card is asserted. The chip, which supports two I/O functions, serves as a standard interface between the PCMCIA bus and the card-side local bus.**

cause a problem because the host computer utilizes that signal to do card testing. Generating an interrupt at the same time could lock up the card or even cause a loss of information.

One final approach, the one the PCMCIA Committee will most likely standardize, makes the PCMCIA card appear to the host-computer system as multiple cards plugged into the single slot. In the proposed specification, there are a series of registers defined as configuration registers. In the original PCMCIA standard, only one set of configuration registers exists for the entire card. With just the one set, there would be a problem if two functions, such as a modem and a LAN, tried to access the registers simultaneously.

The proposed standard puts multiple sets of configuration registers on the card, one for each function that's to be implemented. This minimizes the interaction required to enable or disable a particular function on the card. From a software standpoint, the system software needn't be altered much due to the way it interacts with the card-services layers. Using the new standard, instead of receiving a socket value when the card is inserted, the system gets a combination of socket and function information.

According to Dave Lawrence, president of Ventura Micro Inc., Oxnard, Calif., and chairman of the PCMCIA's Multifunction Working Group, the proposed standard offers a fairly simple interface. "Card designers don't have to worry whether there are multiple functions on the card, which function is currently enabled, what will happen if the second is enabled, and so on," he says.

ADDING REGISTERS

The registers that were added to the set of configuration registers are called the base and limit registers. Those allow system software to accurately program the desired addresses that should appear within the host-computer system's I/O space. The card actually tells the system what address to look for and how many address lines are significant. One important aspect of the specification is that it doesn't limit the amount of functions on a card. The number of accessible functions is determined by the client support.

The proposed standard has been adopted by the PCMCIA's Technical Committee, and the Change Control Board (CCB) gave its stamp of approval. The CCB is a group internal to the PCMCIA Committee that identifies the severity of a proposed standard.

Adherence to the specification requires no system hardware changes. From the system software standpoint, changes must be made to the card services interface, but not the socket services. It's basically an existing enabler that requires some alteration. The enabler is the software that configures the card upon insertion and then releases those resources when the card is removed (the card is typically recognized generically as a class of device, such as a LAN adapter or a modem). The enabler contains readily accessible (instant) data, such as: whether there's a card plugged in; whether the card is configured; and if so, how it's configured. With multifunction cards, there can be twice as much "instant" data.

In designing its CreditCard Ethernet+Modem card, Xircom takes the hardware interrupt and redirects it into other software interrupts using a proprietary driver. The technique works with more than two functions, and is only limited by the amount of available memory. Xircom's designers claim that their technique falls within the boundaries of the PCMCIA multifunction proposal. The CreditCard Ethernet+Modem offers a 19.2-kbit/s fax-modem and a LAN adapter.

Apex Data recently released a similarly configured multifunction card that combines a fax-modem with an Ethernet LAN adapter. Its Combo card employs three different hardware-software interrupt structures to work with different platforms *(see "PCMCIA Fax-Modem and LAN Run Simultaneously," p. 131* PRODUCT INNOVATION IN THIS ISSUE*)*. The best choice of the three is a dual interrupt, which is actually written into the current PCMCIA specification. A Battery-Voltage Dead (BVD) or Status Change signal is employed, which indicates a change must occur in the PCMCIA controller to generate the interrupt.

A newly developed IC that conforms to the proposed standard helps designers implement the multifunctionality. The InfoMover PCM16C00 from National Semiconductor Corp., Santa Clara, Calif., shares the interrupt line using either a pulse or level mode. A PCMCIA interrupt request is asserted whenever the interrupt signal from either function on the card is asserted. The function configuration status registers (FCSRs) indicate

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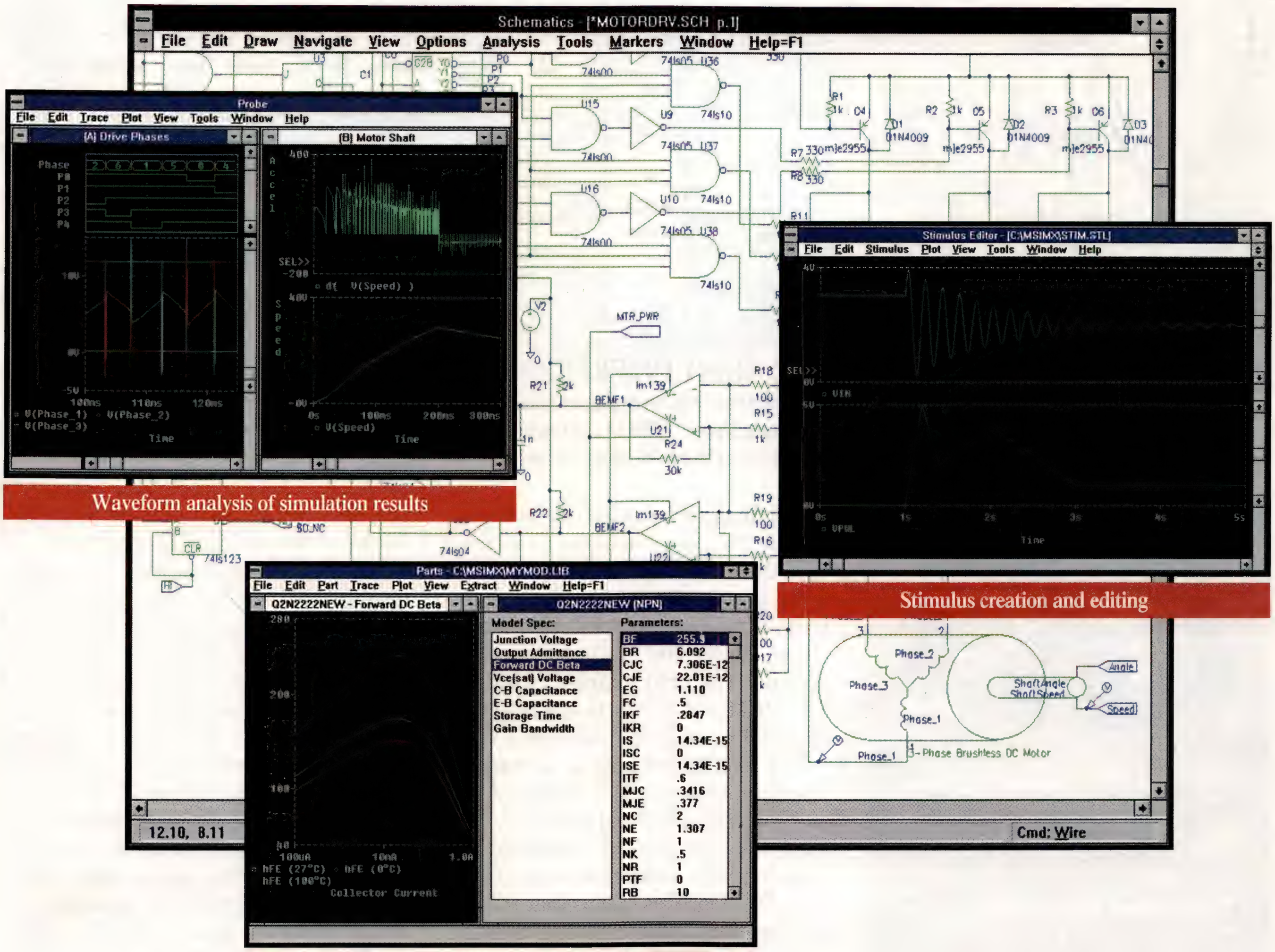
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[A] Drive Phases
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Q2N2222NEW - Forward DC Beta
Q2N2222NEW (NPN)
3-Phase Brushless DC Motor
12.10, 8.11
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Model Spec:
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- Output Admittance
- Forward DC Beta
- Vce(sat) Voltage
- C-B Capacitance
- E-B Capacitance
- Storage Time
- Gain Bandwidth

Parameters:

BF	255.9
BR	6.092
CJC	7.306E-12
CJE	22.01E-12
EG	1.110
FC	.5
IKF	.2847
IKR	0
IS	14.34E-15
ISC	0
ISE	14.34E-15
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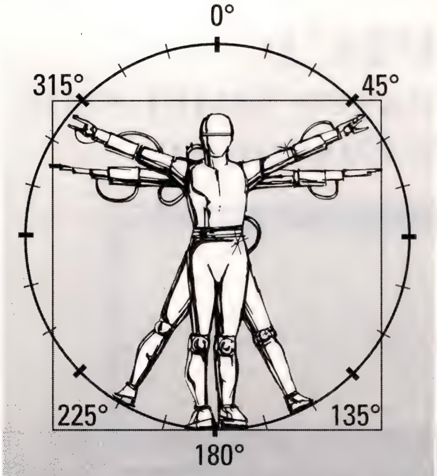

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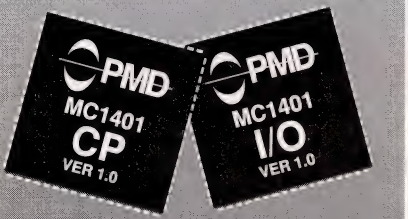

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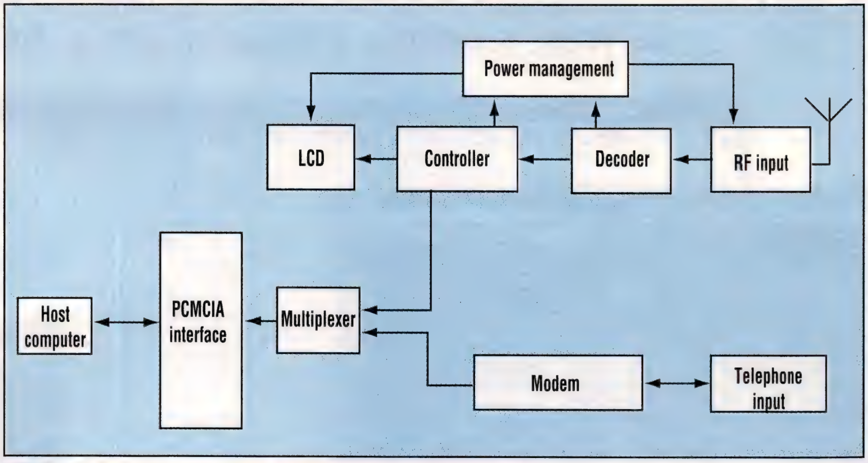

2. MANY INTERFERENCE PROBLEMS had to be overcome in the NovaPak card developed by NovaLink Technologies Inc. The RF circuitry in the multifunction modem/pager PCMCIA card caused the interference. Therefore, in the card's layout, the RF circuitry had to be isolated from the modem circuitry.

which function initiated the interrupt.

"For the host computer to interact with the multifunction card, we had to write a tuple for card services," says Patty Sgambellone, strategic marketing manager for National Semiconductor. "The chip enables multifunction PCMCIA cards to operate with any X86-compatible platform."

The InfoMover acts as a standard interface between the PCMCIA bus and the card-side local bus *(Fig. 1)*. It supports any two I/O functions and memory, with independent control for each function. This means that the user can turn off either or both of the functions to save power. A built-in serial EEPROM interface is compatible with SRAM and flash-memory devices. The chip also supports hot-swapping, meaning that a card can be inserted or removed without having to reboot the system. Operating at either 3.3 or 5 V, the InfoMover is available in a 144-pin thin quad flat pack (TQFP) for $15 each in large quantities.

In addition to the interrupt-request problem, combining functions within a card poses another challenge—the noise from one function must be isolated from the other. To do this, local decoupling of all components is mandatory. However, the 68-pin PCMCIA connector has only four ground and two V_{CC} pins. In addition, component placement must be optimized to ensure minimal routing length. Also, the number of parallel traces must be kept to a minimum to avoid crosstalk. To eliminate external interference, the case of the card acts as a shield between the card and the system.

One particular multifunction card combining a modem and a pager had to overcome many interference problems due to the presence of the RF circuitry. The NovaPak card developed by NovaLink Technologies Inc., Fremont, Calif., required a precise component layout and proper shielding to reduce interference *(Fig. 2)*. In some cases, however, complete shielding of the RF circuits may not be possible because of the limited space. For the NovaPak card, the antenna is housed in an extension away from the EMI generated by the host computer.

Another hurdle that must be overcome in the multifunction-card design process is testing. Sgambellone says, "The challenge of building a multifunction card is that you must develop a program that tests both functions at the same time. That's a significant challenge for card designers. Not only do you have to develop the two independent test programs, but they have to be merged together in such a way that they can operate simultaneously." Typically, card testing is farmed out to a third-party test facility. Consequently, functional testing could add two or three months to the design process. ☐

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HIGHLY	571
MODERATELY	572
SLIGHTLY	573

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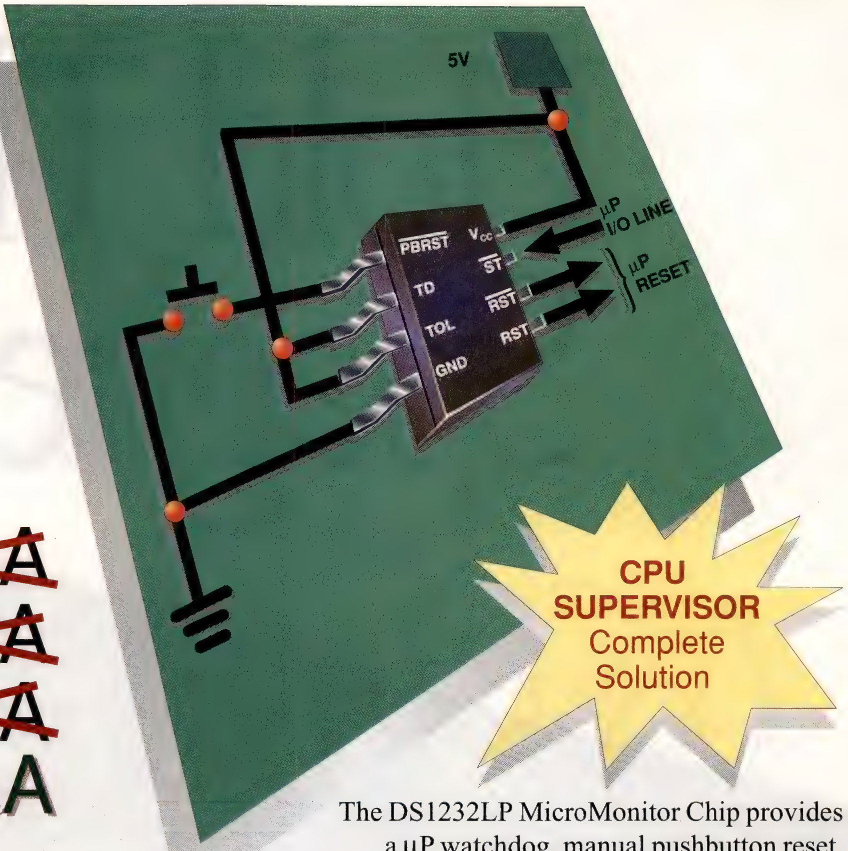
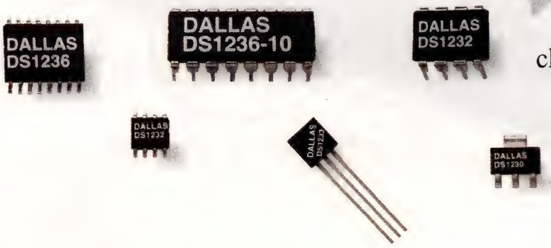


The DS1232LP MicroMonitor Chip provides a µP watchdog, manual pushbutton reset, power-on reset, and power monitor in a 150 mil, 8-pin SOIC package. The DS1232LP is the perfect choice for current-sensitive and size-sensitive applications.



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DS1232 DS1232LP	4.50(S) 4.25(S)	✓	✓	✓	✓				8-Pin DIP 8-Pin SOIC 16-Pin SOIC
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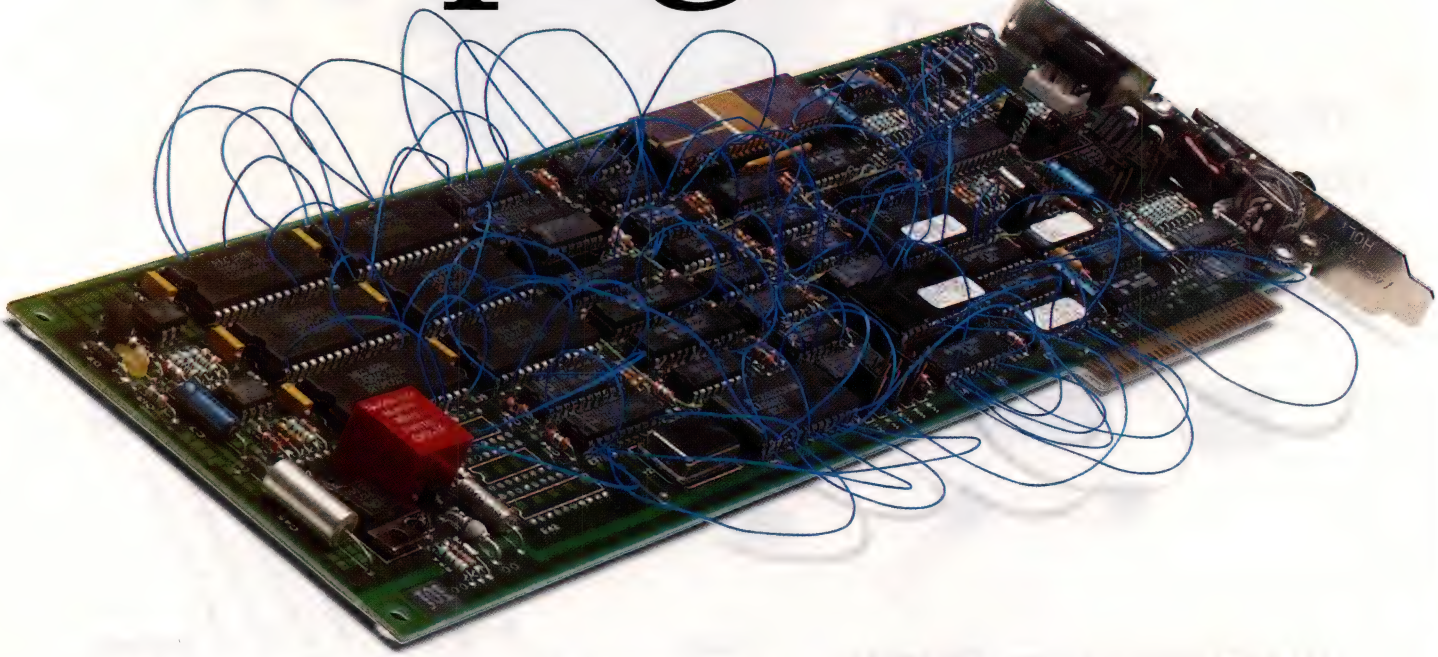

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ITC '94 TARGETS TEST SYNTHESIS

TEST SYNTHESIS JOINS OTHER HOT TECHNOLOGIES ON THE FRONT BURNER AT THIS YEAR'S CONFERENCE AND EXHIBITION.

JOHN NOVELLINO

Celebrating its 25th annual meeting, the 1994 edition of the International Test Conference will focus on "Test: The Next 25 Years" as its theme. Appropriate to this long-term look into the future will be a thorough examination of the emerging technology of test synthesis—the enabling technology for design for testability. The highlight of this examination will be a full-day seminar.

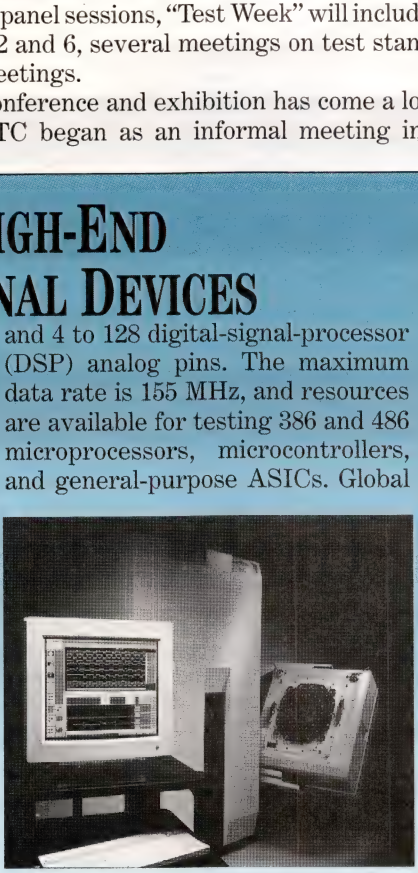
After a two-year diversion to Baltimore, Md., the ITC returns to the Sheraton Washington D.C. Hotel, Oct. 3-5. Along with more than 100 technical papers and nine panel sessions, "Test Week" will include 16 full-day tutorials scheduled for Oct. 2 and 6, several meetings on test standards, and a number of professional meetings.

The conference and exhibition has come a long way since its humble beginnings. ITC began as an informal meeting in 1970 when a handful of test

TESTER HANDLES HIGH-END DIGITAL, MIXED-SIGNAL DEVICES

As a "two-in-one" system, the Duo ATE system tests both high-performance VLSI digital devices and the growing number of high-performance mixed-signal devices going into multimedia computing and communications systems, as well as digital video and audio systems. This dual-architecture design aims at minimizing acquisition and operating costs, and protecting the investment of a customer who needs digital testing now but will eventually require mixed-signal testing.

Duo comes in several versions, ranging from 32 to 512 digital pins and 4 to 128 digital-signal-processor (DSP) analog pins. The maximum data rate is 155 MHz, and resources are available for testing 386 and 486 microprocessors, microcontrollers, and general-purpose ASICs. Global edge-placement accuracy is better than 175 ps.



With the digital platform comes a DSP instrumentation cluster for mixed-signal testing. The DSP video system supplies an impedance-matched, fully differential 16-GHz sampling system designed for a broad range of video applications. The mixed-signal noise floor is 10 nV/√Hz through the audio and video spectrums. Multiple superclocks provide a phase-coherent synchronization architecture for mixed-signal testing and a multiple clock system for asynchronous digital devices or for true parallel testing. System prices depend on configuration.

***Credence Systems Corp.**, 3500 W. Warren Ave., Fremont, CA 94538; (510) 657-7400.*

CIRCLE 601

Booth 704

engineers gathered in Cherry Hill, N.J., to exchange ideas on testing increasingly complex ICs, notes ITC '94 general chair Gerald Gordon. "Now, in celebrating that event, we must prepare our attendees to tackle some even tougher challenges in the next 25 years," he says. "One of the most promising opportunities for meeting these challenges is the emergence of test synthesis."

The show has added several special attractions that will honor its past. For example, attendees will receive a collection of selected papers presented at ITC over the conference's first 25 years.

Test synthesis involves the integration of design and test activities into a synthesis-based design methodology. ITC officials note that developers are working in five basic areas: test-methodology selection, design-for-test (DFT) rule checking, automatic test-structure insertion, automatic test-pattern generation, and test-vector translation for simu-

TEST TOOLS INTEGRATED TO OFFER MIXED-SIGNAL TEST EMULATION

The Dantes virtual test software and Image ExChange test-event simulator have been integrated so that test engineers can verify their complete mixed-signal test package, including the test program and test environment. And, this is possible without waiting for first silicon and without taking time on the tester.

Dantes, developed by Cadence Design Systems, supplies test-capture, rule checking, test-program simulation, ATE code generation, test-fixture design and simulation, and test documentation. The entire test environment—device, fixture, and test instrumentation—can be simulated to verify test operation and performance. Image ExChange allows test engineers to develop and debug test programs on a workstation. The software translates test-program instructions into simulator-compatible events that drive models in the integrated Image/EDA simulator environment.

Dantes costs $80,000 for a single-node license and is available four weeks after receipt of an order. Site licenses for Image ExChange, including interfaces and instrument models specific to the target-design simulator, average $100,000.

Cadence Design Systems Inc., *555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234.*

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ITC '94 TARGETS TEST SYNTHESIS

TESTER MATCHES DATA CARDS TO PIN SPEEDS

Deep submicron CMOS ASICs, microprocessors, and MCMs now can be tested more economically on a system that uses multiple types of data cards to match the performance requirements of the individual device pins. The new Mix-and-Match capability can be added to all high-performance ATS Blazer! test stations.

Because the capability is an enhancement of the ATS Blazer! Plus software, users are able to save money by ordering test stations with the minimum number of data cards needed to handle the device's highest-speed pins. For example, a 200-MHz, 320-pin tester could cost about $1.6 million. But in a typical 320-pin device, only about a third of the pins would run at 200 MHz. By ordering 100-MHz data cards for the remaining pins, a customer could save about 50% in price.

A typical application for the Mix-and-Match capability is in the testing of high-speed microprocessors. As clock speeds increase above 200 MHz, the test fixtures needed for these devices become more complex. These new custom fixtures can easily accomodate the flexible Mix-and-Match software.

Customers under existing ATS Blazer! maintenance contracts will receive the enhanced software without charge. For systems not under such a contract, the ATS Blazer! Plus update costs $10,500. Shipments will begin December 19.

***Integrated Measurement Systems Inc.**, 9525 S.W. Gemini Dr., Beaverton, OR 97005; (800) 879-7117 or (503) 626-7117.*

CIRCLE 604

Booth 104

lators and testers.

The centerpiece of ITC's test-synthesis program is a day-long seminar to be held on Tuesday, Oct. 4. The seminar, organized by Ben Bennetts of Synopsis Corp., will include presentations by industry users, semiconductor manufacturers, and university researchers. One session will discuss the economics of incorporating test features into ICs.

"ITC has always played a leading role in the development of DFT methodologies, such as internal scan, boundary scan, and built-in self-test (BIST)," says Bennetts. "The emerging test-synthesis tools represent an enabling technology for DFT, and we

The Key.

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are offering our attendees a special full-day 'Test Synthesis Seminar' on these tools."

Synthesis is also the subject of the keynote address, a full-day tutorial (all tutorials are available at an extra charge), a panel session, and several technical papers. In addition, a number of developers of test-synthesis tools will participate in the Oct. 2 "Exhibitors Forum."

The keynote speaker, Aart de Geus, president of Synopsis Corp., will discuss "Test—The New Value-Added Field." De Geus notes that test was first believed to be a bearer of bad news, but now has come to be seen as a well-structured discipline of preventive problem management. Things are again changing, he says. Synthesis technology makes possible a diagnostic and automation capability that allows test to add a differentiating product value rather than just minimize cost. De Geus's presentation will review test's potential in the context of key historical and future drivers of electronics design.

The applicable panel session, "How Can I Design a Testable Monster Chip" (Oct. 5, 1:30-3:30 p.m.), will examine the problems of testing chips that can contain several million transistors. Although test solutions must meet tough performance and time-to-market requirements, these very large designs are beyond the capabilities of traditional test approaches. The panelists will look at how test synthesis, BIST, and high-level automatic test-pattern-generation algorithms can solve these problems.

The two technical sessions on test synthesis are "Delay Testing and Synthesis" (session 6) and "Test Synthesis Practices" (session 40). The former includes papers entitled "Fastpath: Robust Path-Delay Test Generator for Standard Scan Design," "On Path-Delay Testing in a Standard Scan Environment," "Automated Logic Synthesis of Random-Pattern-Testable Circuits," and "Transforming Behavioral Specifications to Facilitate Synthesis of Testable Designs." Papers in the latter session include "On Synthesizing Circuits With Implicit Testability Constraints," "A Simulation-Based Protocol-Driven Scan-Test Design-Rule Checker," and "On Achieving Complete Testability of Synchronous Sequential Circuits With Synchronizing Sequences."

Although test synthesis is in the spotlight at ITC '94, other hot test topics aren't ignored. Among those growing in importance in recent years are the IEEE-1149.x family of standards, multichip module (MCM) testing, and current-monitoring, or I_{DDQ} testing.

A panel discussion on "Boundary Scan: It Is Time to Go Beyond Its Boundaries" (session 44) will explore standardization efforts that extend beyond the limits of IEEE-1149.1. Specifically addressed will be designers' needs for shared boundary-scan cell implementations and the use of simpler on-chip controllers. Session

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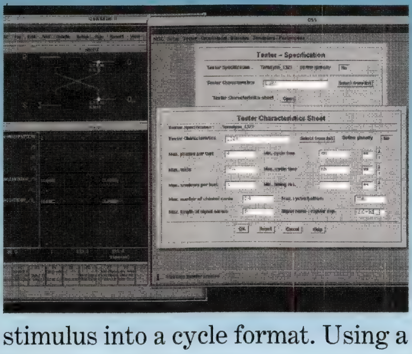
TOOLS CREATE TEST STIMULUS IN DESIGN ENVIRONMENT



A set of software tools integrated into the Mentor Graphics Version 8 environment helps speed up the creation of functional board test programs by creating a cycle-based stimulus. TestArchitect provides a direct link between Mentor's QuickSim design simulator and Teradyne's L-Series board testers.

Because most stimulus created in the design environment isn't cycle-based, it cannot be used on testers. It's difficult, if not impossible, to put stimulus into a cycle format. Using a language called Testcom, however, Test Architect allows engineers to define timing cycles and the digital patterns that use those cycles to produce a usable stimulus. The tools include a rules checker that verifies the tester-compatibility of the stimulus early in the process.

After simulation, the TestArchitect software automatically outputs the Mentor Graphics' databases and simulation results in the LSRTAP format, which is a standard supported by a number of ATE post-processors. The package's post-processor for L-Series testers converts the LSRTAP files to an L-Series test program.

***Teradyne Inc.**, 321 Harrison Ave., Boston, MA 02118 (617) 482-2700.*

CIRCLE 605

Booth 1208

43, a roundtable discussion entitled "Which Backplane Test Interfaces Should I Use?," looks at several approaches to testing multiple modules connected in parallel to the same backplane signals (a multidrop architecture). Participants will examine, explain, and contrast three alternatives: the IEEE-P1149.5 Module Test and Maintenance Bus, the backplane-test-link approach (National Semiconductor's SCAN-Bridge), and the addressable-shadow-port (ASP) approach.

Technical papers on boundary-scan testing will be presented in

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three sessions: "System-Level Applications of BIST, Boundary Scan, and DFT" (session 10), "Boundary-Scan Design Techniques" (session 28), and "Board Test Opportunities and Solutions" (session 37). In addition, Tutorial 13 (Oct. 6) shows how boundary-scan testing facilitates the testing of loaded boards. The tutorial will discuss boundary-scan basics but will emphasize pattern generation for detection and diagnosis of faults within the boundary-scan domain. It also will review commercial tools and products available to support IEEE-1149.1 and other standards being developed.

In the MCM arena, a panel session asks the intriguing question, "MCM Testing: Is It Board Test or IC Test?" (session 15). The panel notes that an MCM manufacturer considers the device a board because it often needs diagnosis and repair. But users think of MCMs as ICs because their defect rates must be as low as that of any other IC. The panel will discuss the pros and cons of different test practices that reflect this dual personality of MCMs.

Two technical sessions target MCMs, specifically: "Known-Good-Die Impact on MCM Testing" (session 2) and "MCM Test Strategies" (session 19). A tutorial scheduled for Oct. 2, "MCM Test Strategies," attacks the problems of complexity and cost of MCM testing. Particular emphasis is placed on testing of bare die; testing of unpopulated substrates; test, diagnosis, and repair of assembled modules; and ways to use MCM-testability techniques beyond assembly testing in areas like board, system, and field testing.

Searching for faults by detecting an increase in quiescent current (I_{DDQ} testing) has become a relatively simple way to test CMOS circuits whose complexity makes access difficult. I_{DDQ} testing will be featured in session 7, "Paving the Superhighway to Ultimate CMOS IC Quality." Other papers slated to address the technique are "A Study of I_{DDQ} Subset Selection Algorithms for Bridging Faults" (session 17), "Is I_{DDQ} Yield Loss Inevitable?" (session 24), and "An I_{DDQ}-based, Built-In Concurrent Test Technique for Interconnects in a Boundary-Scan Environment" (session 28).

Those who want help in actually implementing a testing program can look to tutorial 7, "Current Monitoring (I_{DDQ} testing) for Efficient Detection of CMOS Defects and Faults." The session begins with an overview and proceeds with a description of the physical characteristics and electrical effects of defects and failure mechanisms. It also goes into why I_{DDQ} testing is successful in detecting these effects. Subjects to be covered include pattern generation, selection, and defect grading; recommended DFT schemes; pass-fail limit setting; and ways to diagnose defects. On top of that, the instructors will survey commercially available test equip-

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ment and offer evaluation criteria for commercial software tools.

Besides the keynote address, the opening plenary session will include two invited addresses that should give ITC attendees some idea of where testing is headed in the near future. Robert E. Anderson, president of Omniken Inc., will discuss "A Testing Retrospective and a Questing for Direction." Anderson will examine the major changes in test technologies, philosophies, equipment, economics, and responsibilities caused by changes in electronic devices and subassemblies over the last 25 years. From this discussion, Anderson will draw conclusions and make forecasts.

The other invited address, by Walter Wilson, president of Solectron California, is entitled "Faster, Better, Cheaper: What Does This Mean for the Test Industry?" The slogan "faster, better, cheaper" is more than a 1990s battle cry, notes Wilson. It's a fact of life for anyone involved in manufacturing. He goes on to say that it's critically important for test professionals to understand the concept and its ramifications. Even more important, they must work to ensure that their products will meet these customer demands.

To do this, engineers must study the issues and trends facing the electronics industry, including the effect of new manufacturing and packaging technologies. Specifically, they must know how companies are restructuring to handle three concerns that define the requirements for future test solutions: mass customization, the movement to virtual corporations, and the shift to electronic manufacturing specialists.

Another glimpse into the future will be made in a panel discussion on "Testers and Testing in the Next 10 Years" (session 41). Organizers note how the speed and complexity of both ASICs and commercial ICs challenge the ingenuity of test engineers. Panelists will "gaze into six cloudy crystal balls" in an attempt to forecast what the next 10 years will hold.

New high-speed DRAMs offer much higher data rates than conventional page-mode DRAMs and deliver better system performance. But, say organizers of a roundtable discussion on "Testing High-Speed DRAMs" (session 13), these advantages come at the price of more difficult test problems. The roundtable will address such questions as whether testers can ensure proper DRAM performance, what DFT methods are available for DRAMs, and whether they cost more to test.

The International Test Conference is sponsored by the Test Technology Technical Committee of the IEEE Computer Society and by the Philadelphia Section of the IEEE. ☐

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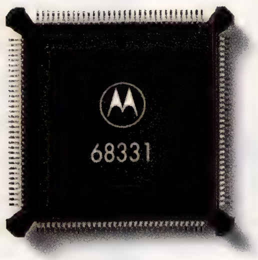

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UPCOMING MEETINGS

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1994 International Conference on Power System Technology, Oct. 18-21. Beijing Continental Grand Hotel, Beijing, China. Contact P.Y. Wang, Electric Power Research Institute, Quinghe, Beijing 100085, China; (86)-1-2913201; fax (86)-1-2913126.

Soft Ferrite Users Conference '94, Oct. 24-25. Westin O'Hare Hotel in Chicago (Rosemont) IL. Contact Magnetic Materials Producers Association, 11 S. LaSalle St. No. 400, Chicago, IL 60603; (312) 201-0101.

Geoworks Technology Summit '94, Oct. 25-26. The Hyatt Regency, Burlingame, CA. Call (800) 524-1857, ext. 1212.

Plastic Optical Fiber Technology & Applications Conference, Oct. 26-28. Yokohama, Japan. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA 02134; (617) 232-3111; fax (617) 734-8562.

1994 International Symposium on Guided-Wave Optoelectronics: Device Characterization Analysis & Design, Oct. 26-28. Polytechnic University, NY. Contact Samantha H. Philips, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3894; fax (909) 562-1571.

1994 5th International Conference on Power Electronics & Variable-Speed Drives, Oct. 26-28. IEE Savoy Place, London, United Kingdom. Contact Jane Chopping, IEE Conference Services, Savoy Place, London, WC2R OBL, United Kingdom; (44)-071-240-1871; fax (44)-071-497-3633.

1994 IEEE Nuclear Science Symposium (NSS), Oct. 30-Nov. 5. Norfolk, VA. Contact Lowell A. Klaisner, Stanford Linear Accelerator Center (SLAC), P.O. Box 4349, Mail Stop 30, Stanford, CA 94309; (415) 926-4463; fax (415) 926-3654.

1994 28th Asilomar Conference on Signals, Systems & Computers, Oct. 31-Nov. 2. Asilomar Conference Grounds, Pacific Grove, CA. Contact Charles W. Therrien, Code EC/Ti, Dept. of Elect. & Comp. Engineering, Naval Postgraduate School, Monterey, CA 93943; (408) 656-3347; fax (408) 656-2760; e-mail: therrien@nps.navy.mil.

18th Space Simulation Conference, Oct. 31-Nov. 3. Hyatt Regency Hotel, Baltimore, MD. Contact Julie Kendrick, The Institute of Environmental Sciences, 940 E. Northwest Hwy., Mount Prospect, IL 60056; (708) 255-1561; fax (708) 255-1699.

LEOS '94, Oct. 31-Nov. 4. Sheraton Boston Hotel & Towers, Boston, MA. Contact Susan Evans, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855; (908) 562-3896; fax (908) 562-1571; E-mail: s.evans@ieee.org.

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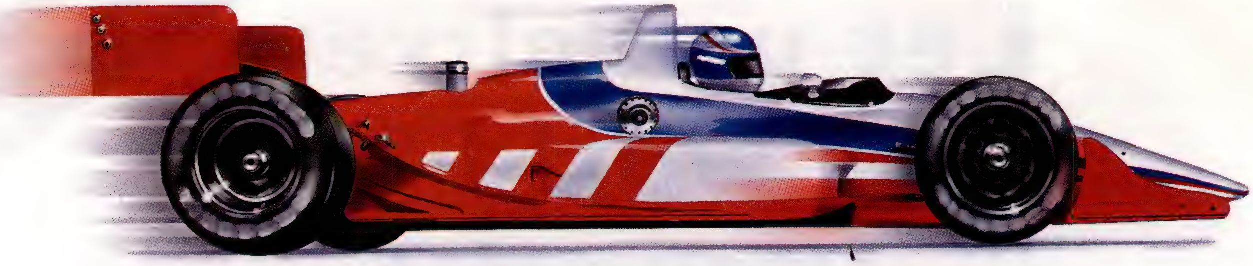

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PRESSURE SENSORS STRIVE TO STAY ON TOP

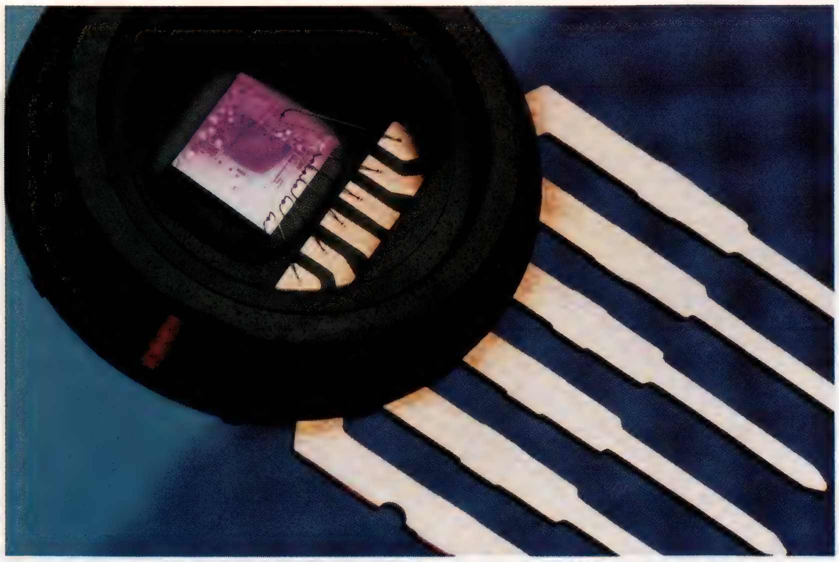
New Silicon Micromachining Techniques And Designs Promise Higher Performance.

BY CHERYL AJLUNI

Research is accelerating into the development of improved silicon micromachined pressure sensors. More novel designs and better fabrication techniques continue to be investigated, heralding trends of increased integration, higher operating temperatures, extended-operating range, improved accuracy and resolution, and the development of more complex structures. It's also enhanced packaging methods and lowered costs. These trends have come about as a direct response to user demands for increased pressure-sensor capabilities. And, as with other semiconductor device areas, designers looking for silicon pressure sensors want "more for less" and are getting it.

Those using pressure-sensing solutions want better control of their systems, which elicits the need for better information from such solutions. This can be done by increasing the number of measurement points, as well as the accuracy of the measurements provided by the sensors. Thanks to the advanced technology of silicon micromachining, pressure sensors are now better equipped to accommodate this trend.

Pressure sensing is one of the most established and well-developed areas of sensor technology. One reason for its popularity is that it can be used to measure various real-world phenomena like flow, fluid level, and acoustic intensities, in addition to pressure. In the automotive industry alone, for example, pressure sensors have been identified for use in 10 different applications *(Fig. 1)*. And, in guidance control and industrial control systems, pressure sensors have long been used for a number of precision pressure measurements.



1. One solid-state sensor application identified for use in automobiles is the manifold-absolute-pressure (MAP) sensor, such as Motorola's MPX4100A. This micromachined device includes full signal conditioning on the same chip as its mechanical-sensing diaphragm, and can be interfaced with microprocessors that have analog-to-digital converters.

Modern pressure sensors are typically silicon-based and are fabricated using the well-established process of silicon micromachining, with capacitance and piezoelectric types being the two most common *(Fig. 2)*. Such sensors are made by bulk micromachining, which involves etching a cavity into the backside of the wafer nearly all the way through the bulk of the silicon. The only part left unetched is a very thin membrane that acts as the pressure-sensing diaphragm. The strain that occurs in the diaphragm, due to the pressure, is monitored by resistors, usually in a Wheatstone bridge configuration. Additional circuitry senses any shift in the resistance and produces a corresponding output that adjusts linearly with the changing pressure.

Though it's not used to create commercially available silicon pressure sensors, surface micromachining also can produce a silicon micromachined sensor. In fact, Analog Devices, Wilmington, Mass., has used surface micromachining to make a low-cost automotive-airbag silicon IC accelerometer with signal conditioning on the chip that can sense ±50 G of acceleration (ELECTRONIC DESIGN, *Aug. 8 1991, p. 45).* Surface micromachining, which etches both the oxide layer and the bulk silicon, is more compatible with standard IC processing steps than bulk micromachining. Thus, it's potentially lower in cost, but, on the other hand, is more complex. Surface micromachining also has been used to make silicon pressure sensors in the laboratory.

In either case, whether it's bulk or surface micromachining, three-dimensional mechanical microstructures are fabricated using standard or modified semiconductor batch-processing techniques. Over the years, silicon micromachining has become more readily accepted as a standard sensor fabrication process. When compared with conventional fabrication techniques, the advantages of silicon micromachining become obvious. Not only does it provide for improved dimensional control, extreme miniaturization, and fully integrated on-chip circuitry, but as a result of batch processing, the cost savings are substantial.

IMPROVED FABRICATION

The Solid-State Sensor and Actuator Workshop held recently at Hilton Head Island, S.C., discussed advances in emerging technologies for sensing. One of the issues actively addressed by both universities and the private sector involved methods for improving sensor fabrication to achieve higher-performance sensing solutions.

Starting with a better wafer material obviously is one way of getting a higher performance pressure sensor. This is exactly the route taken by Paul Aquilino and Paul Zavracky, two scientists at Northeastern University, Boston, Mass. They determined that using silicon-on-insulator (SOI) wafers produced by zone-melting recrystallization (ZMR) as a starting material in surface-micromachining applications offers a number of significant advantages.

To create a ZMR SOI structure, thermal oxide is grown on a bulk silicon wafer. The oxide acts as the insulator in the SOI structure. Although the insulator is typically silicon dioxide, other types of insulators can be substituted. A thin polycrystalline silicon film then is deposited on top of the insulator and capped with an oxide using a chemical-vapor-deposition (CVD) process. The entire structure is placed in a special heating system, which causes the thin silicon film to melt and recrystallize. Once completed, the CVD oxide cap is removed from the structure to reveal the finished wafer.

The process is unique in that it allows the thickness of the thin silicon layer to be specified within the range of 0.1 to 1.0 μm. The thickness uniformity for the wafer is on the order of ±0.015 μm, compared to 0.1 μm for bonded SOI wafers.

During the surface micromachining of a pressure-sensor structure, the thin-film epitaxial layer acts as the diaphragm for the device. Because the diaphragm is isolated from the bulk silicon substrate, it achieves better performance advantages over bulk silicon technology. These advantages include high-temperature operation, higher speed, and a greater packing density. The oxide layer is used as a temporary support structure while a clamp made of polysilicon and silicon nitride is formed. This layer is later removed by an isotropic wet etch, facilitated by including etch ports in the clamp structure or by back-etching through the substrate.

Pressure sensors using the ZMR SOI technique have already been fabricated. They range in size from 50 μm to 2 mm across and offer a pressure range from 250 psi to 10^4 psi. These devices, which can be combined with additional electronics, show promise for low-noise, high-temperature operation.

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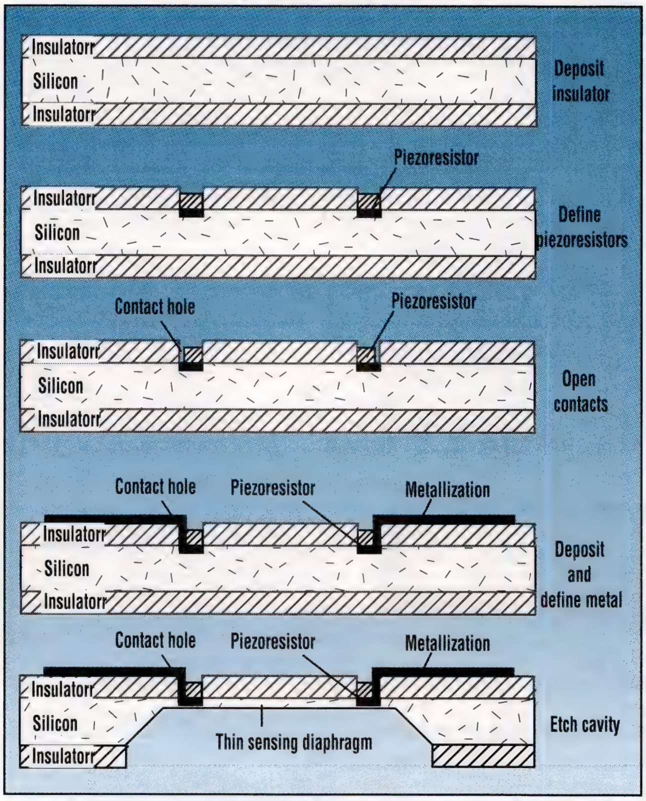
Another way to improve pressure-sensor performance is by using a process that fabricates surface-micromachining-like structures. This technique, known as the wafer-bonding integrated sensor process, was developed through the cooperative efforts of Microsystems Technology Laboratories and the Department of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology in Cambridge. This technique allows electronics to be fully integrated on silicon wafer-bonded substrates in a way that doesn't perturb the IC fabrication process.

The MIT wafer-bonded integrated sensor process consists of three basic steps: pre-IC fabrication, IC fabrication, and post-IC fabrication *(Fig. 3)*. In the first step, a silicon wafer with an etch-stop layer and a silicon handle wafer containing etched cavities are joined together using wafer bonding. The bulk of the first layer is thinned using a modified process that achieves electrical isolation of the mechanical layer from the substrate, producing a wafer with sealed cavities. The wafer looks virtually identical to an unprocessed wafer. The structure then goes through IC fabrication at a standard IC facility. Finally, a pressure inlet port is etched and a capping wafer is bonded using a low-temperature process. These two back-end processes are currently the subject of further research and development.

The wafer-bonding process is marked by two significant features. Primarily, the mechanical layer that results from this process has reliable, reproducible mechanical properties. And, the electronics integration strategy is compatible with standard IC processes and equipment. Effectively, the wafer-bonding process allows for the full integration of electronics monolithically with high-quality micromachined devices.



2. This sequence of events is typically required for the fabrication of a simple micromachined silicon pressure-sensor chip.

NEW SOLUTIONS

While many researchers are focusing on ways to improve fabrication techniques, others are developing new types of pressure sensors that will eventually be utilized as sensing solutions in various different engineering systems. Many of these devices integrate advanced functions and offer increased flexibility. Though they represent only a few of the different types of pressure sensors, they succeed in illustrating how the application of pressure sensors is changing.

One of the more unique applications of a pressure sensor is the brainchild of researchers at the Berkeley Sensor and Actuator Center, along with the Departments of Mechanical Engineering and Electrical Engineering and Computer Sciences, Berkeley, Calif. Realizing that a microphone is basically a pressure sensor that can detect airborne sound pressures ten orders of magnitude lower than ambient pressure, they developed a micromachined piezoelectric cantilever transducer that can work as both a microphone and microspeaker.

Typically, pressure-sensor designs integrate a diaphragm that's clamped on all four edges. The microphone/microspeaker device, though, is unique in that it employs a cantilever diaphragm. This allows for a more compliant diaphragm and eliminates the tension found in clamped diaphragms, which can lead to decreased transducer response. Subsequently, the microphone exhibits a sensitivity of 2 mV/microbar in the low-frequency range, which rises to 20 mV/microbar at the lowest resonant frequency of 890 Hz. This is much higher than is possible with older microphones and their micromachined diaphragms. The microspeaker output sound-pressure level is 75 dB at 890 Hz in a 2-cm^3 coupler with a 4-V (zero-peak) drive. At 4.8 kHz with a 6-V (zero-peak) drive, the sound-pressure level increases to approximately 100 dB. The 2000-by-2000-by-3-µm cantilever has a zinc-oxide (ZnO) piezoelectric thin film on a supporting layer of low-pressure CVD low-stress silicon nitride.

An interesting aspect of this device and the most challenging part of its fabrication is the technique used to produce the flat multilayer cantilever. In the past, these devices were significantly curled upward or downward, due to the gradient of the residual stress of the silicon-nitride layer and the high residual compressive stress of the ZnO layer, respectively. Researchers determined that the upward curl could be eliminated by patterning the ZnO so that it's not contiguous to the silicon support portion of the cantilever. They also found a method for reducing the downward curl.

A layer of silicon-nitride with a 6:1 reactant-gas ratio is first deposited to form a diaphragm. After

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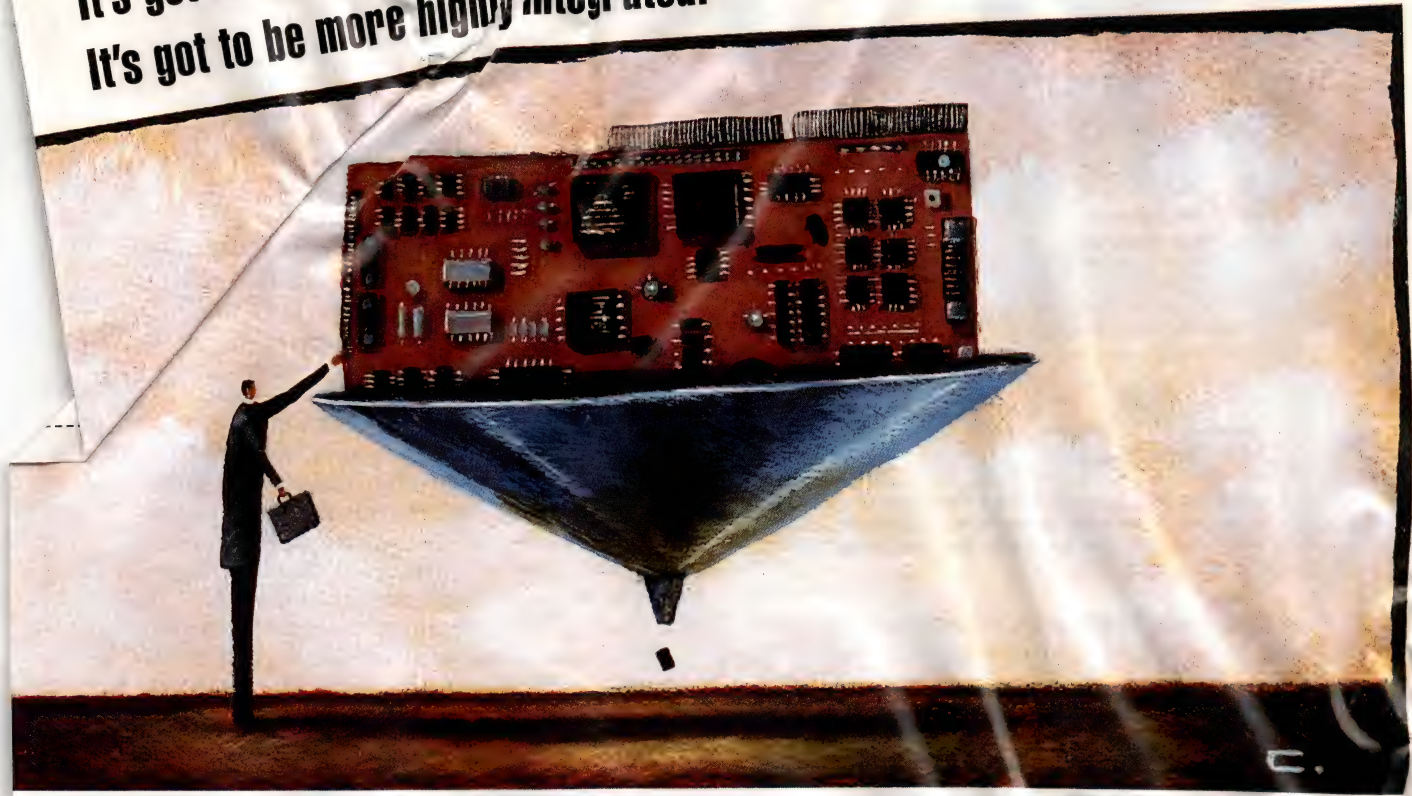

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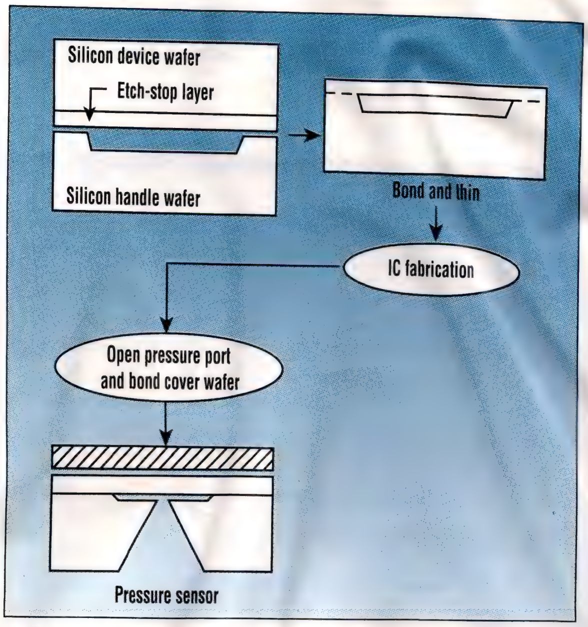

3. By using this integrated technique, pressure sensors and other electronics can be fabricated on the same silicon wafer. Developed at MIT, the technique is based on the wafer-bonded integrated sensor process.

bulk-micromachining, a second low-stress silicon-nitride layer with a 4:1 gas ratio is deposited. The second-layer deposition occurs on both sides of the original diaphragm, causing the stress gradients to become symmetric. During the second-layer deposition, the first layer is annealed and its stress distribution is negligible. The result is a flat cantilever.

Another novel pressure-sensor design comes from a joint venture between the Honeywell Technology Center, Bloomington, Minn., and the University of Wisconsin's Center for Applied Microelectronics in Madison. Their highly integrated design is based on the use of resonant microbeam technology. It combines a sensing element_a precision polysilicon microbeam structure_with conventional digitizing circuitry on the same wafer.

essure sensors are packaged in many forms. essure transducer, created by Honeywell, is pack- because of its reliability in harsh environments. des digital-signal processing circuitry.

With resonant sensors, the output is in the form of a robust sinusoidal signal whose frequency changes with pressure. The resonant microbeam sensor, therefore, is termed quasi-digital because with the use of a high-frequency clock, its output can be easily converted to a digital form. Interconnection with digital control system is possi[illegible]rough electrical or optical means, and provides for operation in a number of harsh environments.

In this particular design, strain-sensit[illegible]cal-grade polysilicon resonators are fabrica[illegible]lithically on silicon-pressure diaphragms with ani[illegible] vacuum-sealed cavities for differential or abs[illegible] pressure sensors. Combining the best of fine-grain[illegible] polysilicon, advanced surface micromachining, and reactive sealing technologies, pressure sensitivity of nearly 4000 counts/s per psi have been obtained on a 10-psi device with a frequency of 233 kHz.

In addition to high-performance characteristics, today's precision pressure applications now require smart transmitters that provide a calibrated, temperature-compensated output in a specified format. In the case of resonant sensors, it's possible to integrate the oscillator electronics, which address these issues, at the chip level, using simple analog electronics. Then, because the electronics are included in the package as opposed to on the sensor chip, a separate microcontroller chip can be interconnected to the sensor to control the electronic functions. This allows much greater flexibility and faster time-to-market than if they were to be combined on the same chip. Subsequently, separate manufacturing processes can be employed for each chip, without compromising sensor design, IC design, or processing, in trying to achieve a merged process. While this method is still being developed, other discrete surface-mount elements are being used for oscillator electronics.

Present high-performance pressure-sensing requirements in applications ranging from transportation to avionics dictate that pressure must be measured with high resolution and sensitivity, and that the sensor must have a large dynamic range. The conventional method of addressing these issues involves the use of a very sensitive capacitance or piezoresistive sensor. Now, however, another option is available that promises to surpass these conventional devices in terms of sensitivity, size, and dynamic range.

That option, devised by the scientists at the Center for Integrated Sensors and Circuits at the University of Michigan in Ann Arbor, utilizes the tunneling current between a tunneling tip and a movable diaphragm or beam to sense deflections. Not only can tunneled-based sensors produce sensitivity equal to, if not greater than, capacitance sensors, but they do so without the need for either super-thin or large-area diaphragms or beams. The subsequent effect is that sensor fabrication becomes easier and potentially improves uniformity and yield.

A tunneling-based sensor is developed using a boron, etch-stop, bulk-silicon, dissolved wafer proc-

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ess. In this process, a cantilever beam is formed that supports a tunneling tip and a thin pressure-sensitive diaphragm. Both the tip and diaphragm are attached to a glass substrate. The wafer that forms the diaphragm also acts as a counter electrode for sustaining a tunneling current to the tip on the beam.

The completed sensor operates in two modes: the constant-voltage open-loop mode, where the change in tunneling current is used to provide an indication of pressure change; and the constant-current closed-loop mode, where the feedback voltage between the beam and deflection electrode can provide an indication of pressure change. By changing diaphragm and beam dimensions, the sensitivity and dynamic range of a tunneling-based sensor can be varied over a large range.

One sensor developed using this technique employs a 700-by-700-by-3.5-μm diaphragm and a straight beam that's 3.5 μm thick. It can measure pressures from 1 mTorr to 10 Torr and provides a current sensitivity to pressure of 0.2 nA/mTorr. Thanks to the flexibility of the technology and design process, any number of low-voltage tunneling-based pressure sensors with different designs (different dimensions and thicknesses for the diaphragm and support beam) can be developed.

MORE INTELLIGENCE

Several companies also are continuing to produce commercially available pressure sensors with greater intelligence. For example, the Semiconductor Products Sector of Motorola, Phoenix, Ariz., and Honeywell's Solid State Electronics Center, Plymouth, Minn., developed such sensors. Both devices have been fully tested and are available.

Motorola's low-pressure sensor can sense full-scale ranges down to 1.5 in. of water, at an accuracy and resolution within 1% of the full-scale reading. The module consists of a single-chip, signal-conditioned pressure sensor and an on-chip temperature sensor. Additional subsystems include power-supply rejection circuitry, an MCU oscillator circuit, a low-voltage inhibit supervisory voltage-monitoring circuit, a 5-V ±5% linear voltage regulator, and an on-board 8-bit microcontroller. The microcontroller handles software calibration, software temperature compensation, and dynamic-zero capability. Besides measuring pressure with high accuracy, the module has a digital output that's compatible with Motorola's Serial Peripheral Interface (SPI).

Honeywell, on the other hand, came up with a microprocessor-based precision pressure transducer (PPT). The modular PPT, based on silicon-sensor technology, is fabricated using Honeywell's patented silicon process and special assembly techniques, which result in extremely stable and repeatable characteristics *(Fig. 4)*.

The PPT offers total accuracy that's within 0.1% of full scale over the temperature range of –40 to +85°C. It's available with pressure ranges of 0 to 1 psi, 0 to 15 psi, 0 to 100 psi, and 0 to 600 psi. Also available in absolute, gauge, or dry-gas differential configurations, the PPT can interface directly to systems requiring a high-level analog 0- to 5-V or RS-232 output without additional circuitry. Furthermore, it has user-selectable features such as addressibility, resolution, readout, and a sampling rate that automatically increases for rapid pressure changes.

STANDARDS ARE NEEDED

The outcry for meaningful pressure-sensor standards continues to get louder. Heeding that call, the standards body of the IEEE Instrumentation and Measurement Society TC-9 Committee is sponsoring the development of a smart sensor bus. This effort, led by Janusz Bryzek, executive vice president of Lucas NovaSensor, is currently working on revision 5.0 of a draft standard entitled "Microfabricated Pressure and Acceleration Technology." A subgroup of this committee is working on a separate document dealing with standards for calibration and test procedures. It's in the revision stage as well. The IEEE also is working on a joint effort with the National Institute of Science and Technology (NIST) to develop standardization within the sensor industry. These groups are focusing on interface and protocol standards to aid system designers and manufacturers, among other issues.

Ultimately, standards let designers take advantage of new sensor technologies more readily. One key aspect of such standards is an ability to communicate with and control these devices. During the last several years, various organizations worldwide have been developing smart-sensor bus protocols and products to address this need. As designers look for ways to efficiently handle remote intelligent devices, though, the debates over protocol standards seems to stand in the way.

Overall, these efforts did bring about some interesting options, but a uniform standard has yet to be adopted. One recently completed standard is the Fieldbus, which comes out of Brazil-based Smar Research Corp. It takes full advantage of advanced communications and control capabilities and works with the WorldFIP and ISP protocols.

Fieldbus is a digital communication bus to interconnect field devices with a control system, and encompasses a comples seven-layer structure. Its prime advantages include low-cost cabling, installation, operation and maintenance, prompt information about field-device fault diagnostics, increased system robustness, and better accuracy of measurement and control signals. Future developments of this and other options will focus on ways to provide a system general enough to eventually be adopted as an industry standard. ☐

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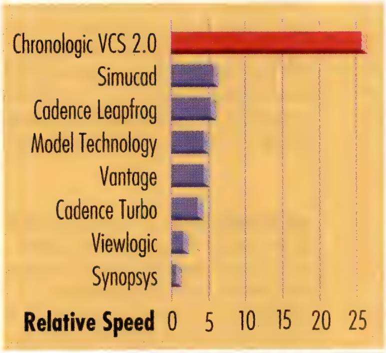

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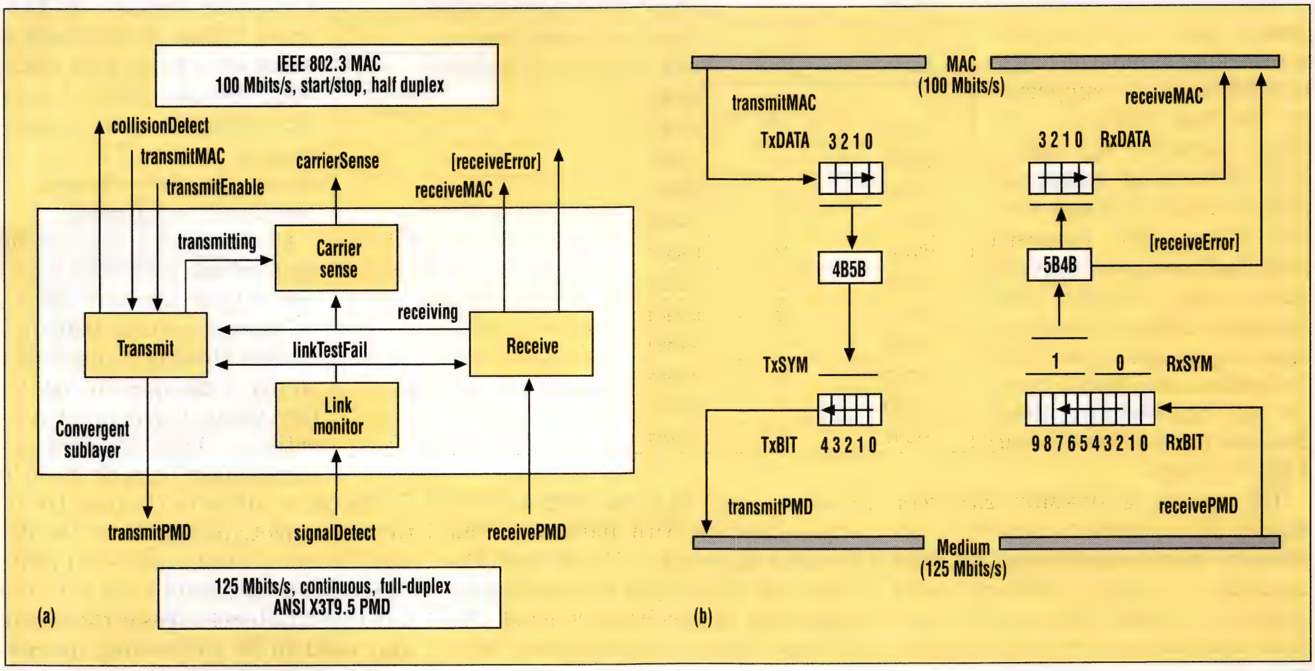
The newest generation of networking applications built around emerging standards require much more performance from digital logic than previous systems. Gate arrays may have the required speed, but don't possess the flexibility needed to support multiple design iterations. The current generation of speedy field-programmable gate arrays (FPGAs) can supply performance while also providing the flexibility needed to make frequent design changes. FPGAs can accelerate the design of high-speed networking equipment and thus allow for quicker market development, hastening the adoption of emerging standards.

Several new standards are being developed to increase network bandwidth at the desktop. An order of magnitude increase in bandwidth is needed to satisfy the desktop applications' demand for more data at faster rates. Current contend-



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ers for the next-generation interconnect standard include FDDI over twisted pair, 100Base-VG, Fibre Channel, P1394, Scalable Coherent Interface, Quickring, ATM, HiPPI, and 100Base-X. All of these standards provide for much higher data rates to network-hungry applications. However, all of them may undergo changes prior to full market acceptance.

Because of the complex nature of these applications, it's usually necessary to build complete networks of perhaps hundreds of nodes to prove out a standard. Invariably, changes need to be made to allow for compatibility with existing equipment and the previous generation's “warts.” In fact, many of these changes only show up when detailed diagnostics are run. Ideally, the first implementation of these application types use additional logic to help debug the overall system. The quick turnaround times available with FPGAs makes it possible to design-in this logic when required, and then easily change or remove it.

One of the more recent entrants into the high-speed networking standards battle is 100Base-X. It's supported by the Fast Ethernet Alliance, sponsored by several key networking companies such as Intel, National, Sun, and 3Com. The proposed standard is representative of many types of digital logic functions facing high-speed network designers, and will be used as a real-world example of implementing these fast moving standards using FPGA devices.

The emerging 100-Mbit Ethernet market is expected to mushroom as network performance requirements continue to grow. Network users probably doubled between 1991 and 1994, and networks will need to provide these new users with just as much, if not more, bandwidth. A high-speed Ethernet network could solve users' bandwidth problems, and maintain compatibility with current equipment and software.

The 100Base-X proposal employs two established networking standards to support the 100-Mbit data rate—ten times the 10-Mbit rate of the current Ethernet standard. The media-access-control (MAC) layer is kept the same as in the current Ethernet standard with 100Base-X, but the data rate rises to 100 Mbits/s. Because the MAC layer was defined independent of performance level, this increase can be accomplished relatively easily. In addition, the proven behavioral dynamics of the Ethernet MAC can be retained. The only change required involves reducing the physical network span by 1/10 of the 10-Mbit/s version. This results in a span of about 250 meters.

This reduced span fits well within the current structured wiring methodologies. Floor wiring in modern installations of Ethernet, such as 10Base-T, is built in a star with a centralized wiring closet. Cable runs are less than 100 meters. For LANs, this results in a hub/station architecture with interconnections of less than 100 meters.

At the physical layer, 100Base-X leverages off the proven FDDI standard for 100-Mbit/s communications using a full duplex 125-Mbit/s physical-media-dependent (PMD) sublayer. As a result, it supports fiber-optic, shielded twisted-pair, and unshielded twisted-pair wiring. Combining the MAC layer of Ethernet with the PMD layer of FDDI requires a convergent sublayer (CS). Using the CS, 100Base-X maps the PMD's constant signaling system to the packet-oriented half-duplex system imposed by the Ethernet MAC. This is similar to a popular variant of Ethernet, 10Base-T, which also is based on a full-duplex channel. The convergent sublayer for 100Base-X can be implemented using FPGAs to speed the development of 100Base-X equipment.

Obviously, raw speed is the first criteria for FPGA selection in these applications. An additional criteria that may be less obvious is the ability to make changes to the design without changing pin locations. This requirement comes about from the need to fix the pin locations on the board prior to the complete design. Once the design is completed, place-and-route needs to be successful even with the fixed pins. Later changes in the design also need to be successfully placed-and-routed within these constraints. Moreover, timing changes must be minimized so that high performance levels are still met. Actel antifuse

SYMBOL CODING

Code Group	Symbol	Interpretation
		Data
11110	0	hex binary 0 0000
01001	1	1 0001
10100	2	2 0010
10101	3	3 0011
01010	4	4 0100
01011	5	5 0101
01110	6	6 0110
01111	7	7 0111
10010	8	8 1000
10011	9	9 1001
10110	A	A 1010
10111	B	B 1011
11010	C	C 1100
11011	D	D 1101
11100	E	E 1110
11101	F	F 1111
		Idle
11111	I	Idle, used between packets
		Control
11000	J	First of start-of-packet delimiter
10001	K	Second of start-of-packet delimiter
01101	T	First of end-of-packet delimiter
00111	R	Second of end-of-packet delimiter
		Invalid
00000	V	Invalid
00001	V	Invalid
00010	V	Invalid
00011	V	Invalid
00100	V	Invalid
00101	V	Invalid
00110	V	Invalid
01000	V	Invalid
01100	V	Invalid
10000	V	Invalid
11001	V	Invalid

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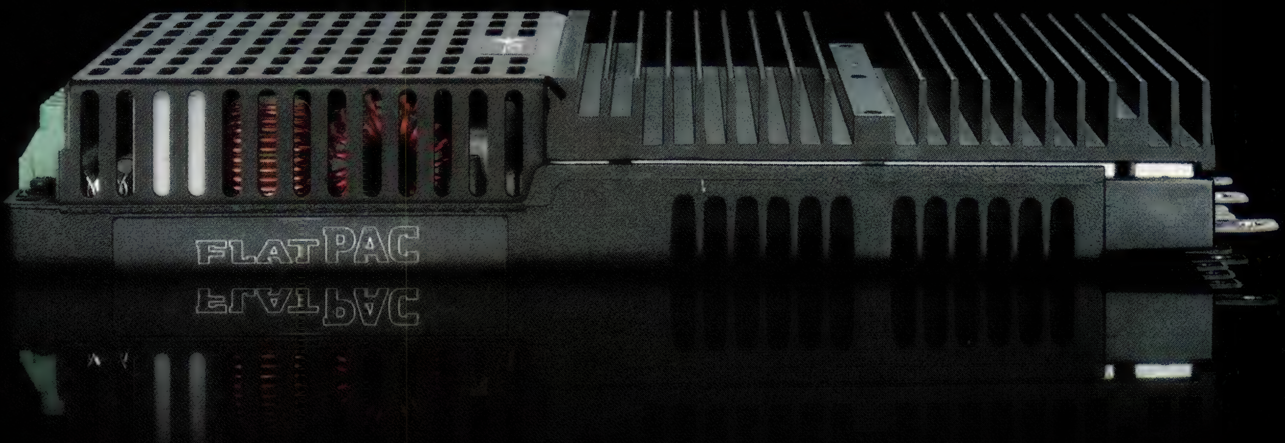

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FPGAs, which have an abundance of routing resources, high capacity, and high speed, can satisfy these key objectives *(see "The ACT3 FPGA family," left)*.

The convergent sublayer for 100Base-X receives 125-Mbit/s data from the PMD *(Fig. 1a)*. The 125-Mbit/s physical data rate employs five bits to encode 16 data combinations and the signaling symbols required to indicate the start and end of the data packet. In addition to the 16 valid data bits, five special control signals are used to indicate start-of-packet (J followed by K), end-of-packet (T followed by R), and Idle (I).

All other 5-bit combinations are Invalid, and represent channel errors or repeater collision artifacts. Thus, the physical line will Idle until the start of a data packet is indicated by a J symbol followed by a K. Data symbols come next, with the end of data being indicated by a T symbol followed by an R. The Idle symbols come immediately after that.

The convergent sublayer's job is to extract the data symbols from the packet and provide it as a data-only packet to the MAC. As a result, the MAC never receives Idle, JK, or TR symbols. When receiving, the CS reverses the process, encapsulating and encoding the data from the MAC for transmission by the PMD.

A functional breakout of the CS and the associated data-flow model shows that the Receive function generates receiveMAC and receiveError for the MAC based on receivePMD *(Fig. 1a, again)*. The Transmit function accepts transmitMAC and transmitEnable from the MAC, and generates transmitPMD. CollisionDetect is generated by the Transmit function, based on the transmitEnable and receiving signals.

The carrier-sense function asserts carrierSense when the convergent sublayer is either transmitting or receiving, based on the two corresponding internal signals generated by the transmit and receive functions. Link monitor generates linkTestFail based on the PMD's signalDetect. Actually, linkTestFail is an internal signal not used by the MAC, and is optionally used by a network-management entity.

During data flow from the MAC to the PMD, the transmitMAC signal in-

THE ACT3 FPGA FAMILY

Actel's ACT3 FPGA family is built with a channeled gate-array-style architecture. I/O macros are located on the periphery of the device, and the core contains alternating stripes of logic modules and routing channels *(Fig. A)*. The logic module implements combinatorial and sequential functions, while the channels connect module outputs to module inputs.

Actel's patented PLICE antifuse allows for a low-impedance connection, and is a major reason for the predictable performance of the ACT3 family that achieves 7.5 ns clock to out (pin-to-pin) and over 150-MHz clock rates. The ACT3 logic module can implement functions with up to eight inputs. One half of the modules include a D-type register to support sequential logic *(Fig. B)*.

The combinatorial logic module can be used to create a wide variety of logic gates by connecting input signals and logic True and False signals to the module inputs. For example, a five-input OR function can be implemented by connecting the five input signals and three logic HIGHs *(Fig. B, again)*.

Over 200 different logic gates can be implemented by using the ACT3 logic module in this same way. The sequential module adds a D-type flip-flop to the combinatorial module output, which also makes it possible to create sequential functions in a single module.

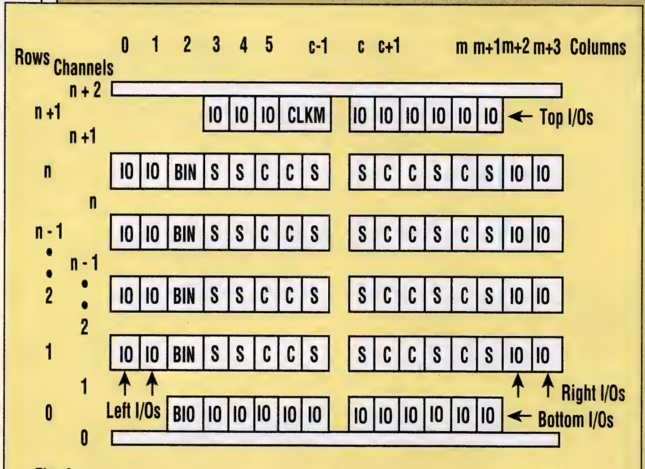
Rows
Channels
0 1 2 3 4 5 c-1 c c+1 m m+1 m+2 m+3 Columns
n + 2
n +1
n +1
n
n
n - 1
n - 1
2
2
1
1
0
0
IO IO IO CLKM IO IO IO IO IO IO
Top I/Os
IO IO BIN S S C C S S C C S C S IO IO
BIO IO IO IO IO IO IO IO IO IO IO IO
Left I/Os
Right I/Os
Bottom I/Os

Fig. A

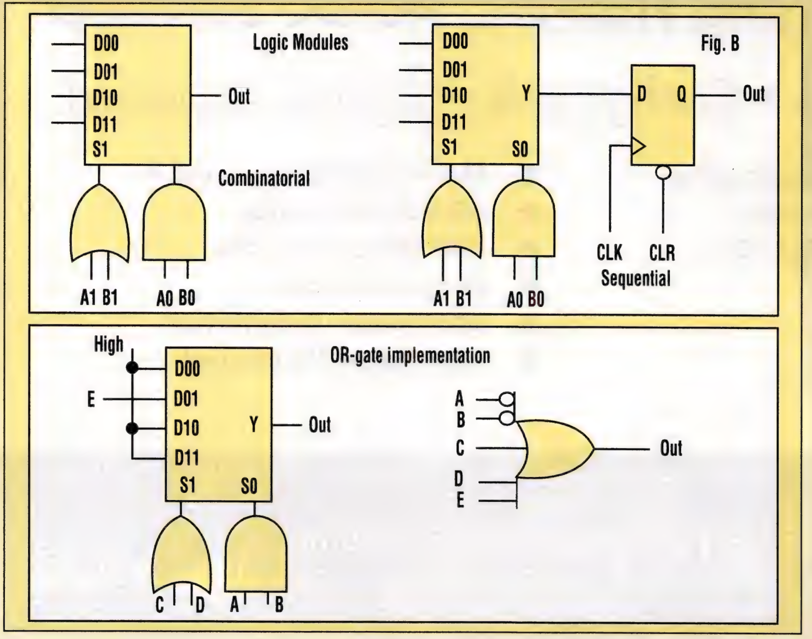

Fig. B

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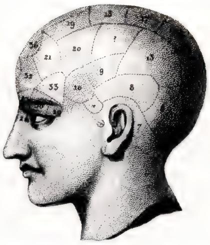

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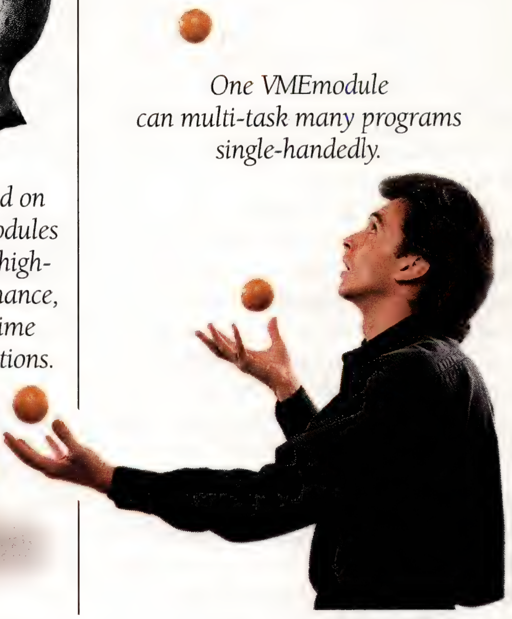

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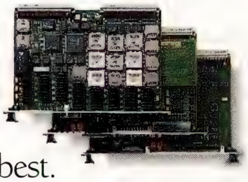

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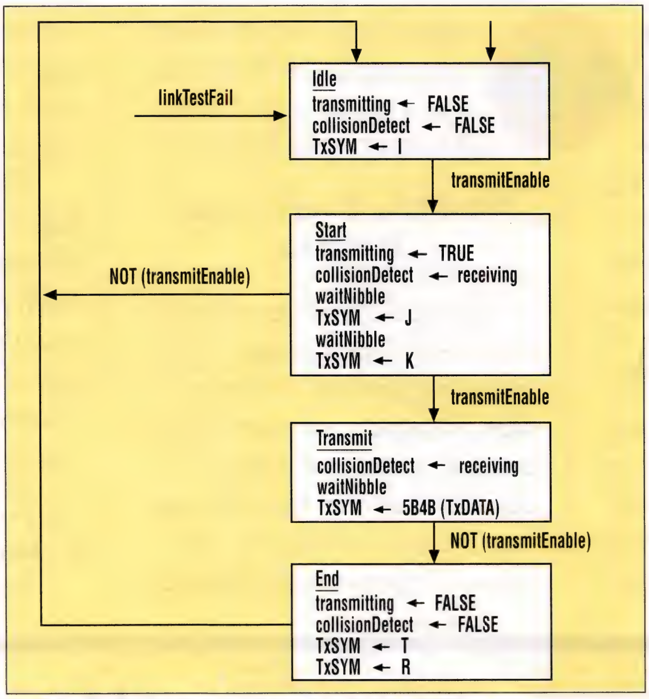
dicates MAC data is available and is registered internal to the convergent-sublayer logic *(Fig. 1b)*. The four data bits are converted to five bits prior to transmission on the 125-Mbit/s PMD. Note that TxDATA, TxSY, and TxBIT are all different views of the same data at different data rates.

When data is received from the PMD, the convergent sublayer needs to shift in the serial data, detect the start of packet, align data on a symbol basis, and convert from 5- to 4-bit encoded data. The actual 100-Mbit/s data stream is forwarded to the MAC with the required start and stop indicated by receiveMAC and carrierSense.

The state diagram for the transmit state machine uses conventional representations *(Fig. 2)*. State names are underlined. The actions specified are assumed to be instantaneous, although for simplicity, some time-sequenced events are contained in single states. Unconditional state transitions are unleveled. Conditional state transitions occur when explicitly shown by the accompanying condition; the state is repeated until some transitional condition is detected. States are atomic in that conditions get evaluated only at the completion of the state's actions. Transitions shown without source states, notably linkTestFail, are evaluated at the completion of every state, and take precedence over other transition conditions.



2. A STATE DIAGRAM FOR THE transmit state machine uses conventional representations in which states are labeled with an underlined title.

The transmit state diagram begins with the Idle state. The transmitting and collisionDetect signals are initialized as False, and the Idle symbol is continuously supplied to the PMD. When the MAC has data to transmit, it asserts transmitEnable and the Start state is entered. The transmitting signal is asserted, indicating to the carrier sense function that data is being transmitted. In addition, collisionDetect is set to the level of the receiving signal.

The receiving signal comes from the receive function. A collision has occurred if it also is asserted. The waitNibble function synchronizes the MAC data with the PMD clock, and the first eight bits of the MAC preamble are replaced with the /J/K/ symbol pair. If transmitEnable becomes False, the machine transitions back to Idle. If transmitEnable stays asserted, the next state becomes Transmit.

During Transmit, collisionDetect is still set to receiving. The MAC data (TxDATA) is encoded using the 5B4B function. Encoding continues until transmitEnable is deasserted. Once transmitEnable is deasserted, the machine transitions to End.

In the End state, transmitting and collisionDetect are both False. The /T/R/ symbols are transmitted to indicate the end of data, and the machine moves to the Idle state. The assertion of linkTestFail (by the link monitor function) causes an immediate transition to the Idle state, and takes precedence over any MAC request.

The design of the key transmit function will show some common design techniques employed in high-speed FPGA applications. The entire design is too large to cover completely, but the selected function shows the type of techniques used in FPGAs.

Basically, the transmit block provides the requested symbol data to the PMD at a 125-Mbit/s serial rate. This requires the 4-bit data word be encoded using a 4B5B encoding table *(see the table)*. In addition, it must be shifted out using the 125-MHz clock. The serial data stream must be encapsulated using the leading /J/K/ symbol pair and trailing /T/R/ symbol pair. When data isn't transmitting, the Idle symbol must be sent.

In the datapath portion of the transmit block, the main flow of data comes from the MAC at 25 MHz with a 4-bit-wide data word and a control signal that enables transmission *(Fig. 3)*. When MAC data isn't being transmitted, the convergent sublayer sources continuous Idle symbols to the PMD. But when the transmitEnable signal becomes active, a /J/K/ symbol pair is transmitted to indicate the beginning of a data packet. MAC data symbols follow, and are encoded into 5-bit symbols using the 4B5B encoding scheme *(see the table, again)*. Then, the end of MAC data is indicated by the transmitEnable signal going inactive. Finally, a /T/R/ symbol pair is inserted at the end of the data packet and the CS logic returns to transmitting the Idle symbol.

Implementing these transmission functions involves selecting six different symbol sources for PMD data: the Idle, J, K, T, or R symbol, in addition to the 4B5B-encoded MAC data. Also, a TestData input can be used to provide raw unencoded data to the PMD for diagnostics and testing.

This selection is accomplished via the multiplexer in front of the output shift register. One multiplexer selects among the I, J, and K symbols, or another multiplexer output. The other multiplexer selects between the T or R symbols and encoded MAC data. An additional path around the encoder that supplies raw (unencoded) data to the PMD is used for system test and diagnostics. It's the only way for known errors to be injected into the system, simulating collision remnants and exercising the boundary conditions of the standard.

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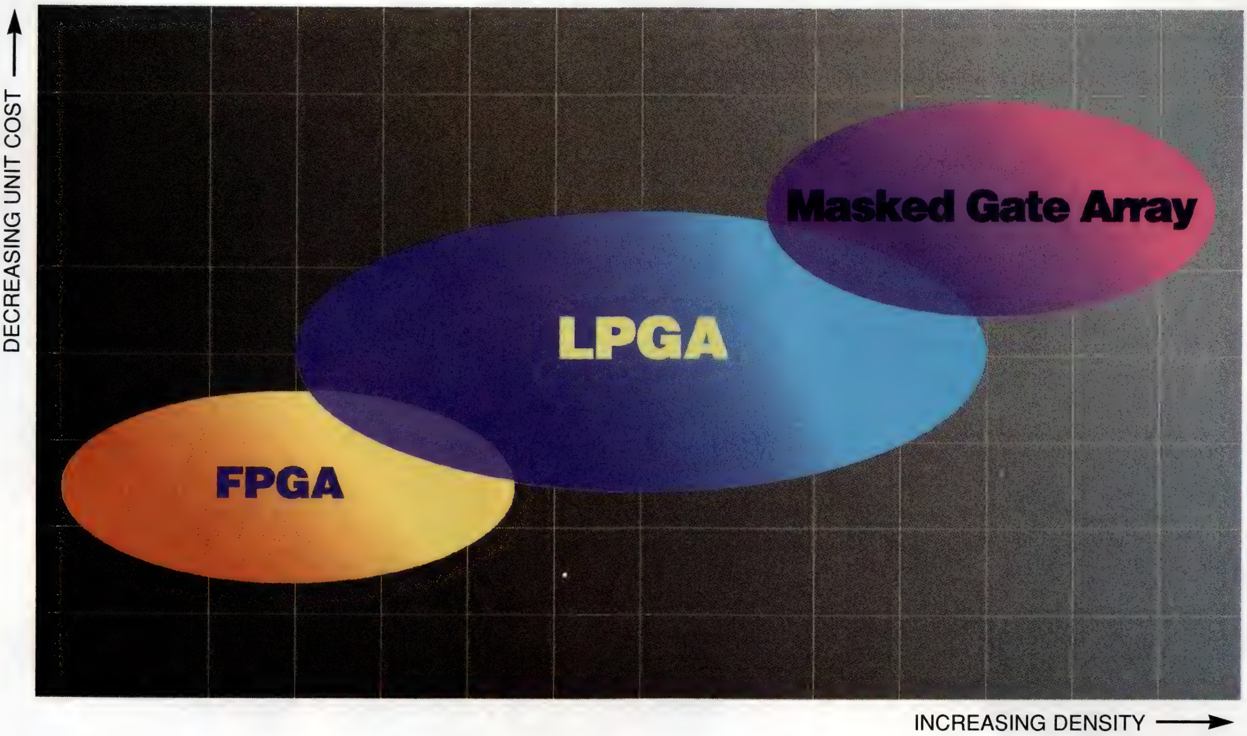

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multiplexers in one logic module. Upon inspection, it's revealed that the path through the multiplexer tree will require only two module delays, and thus will easily meet the 25-MHz performance requirement. The 4B5B encode block also requires just two logic modules, and can be designed via schematics or equations. Equations can be automatically compiled using Actel's ActMap tool, and then incorporated into the schematic. The input equations are shown in Figure 3.

The receiving state diagram consists of two separate sets of states *(Fig. 4)*. Idle, Scan, Carrier, and Align states are pre-aligned and operate on the raw input bits using RxBIT. All other states are aligned and run on the input data stream as symbols (RxSYM). Output data, known as RxDATA, is sent directly to the MAC in these states.

The receive state diagram begins with the Idle state. Both the receiving signal and the optional receiveError signal are initialized to False. Scan is entered next, and the waitBit function synchronizes the machine to the received data stream.

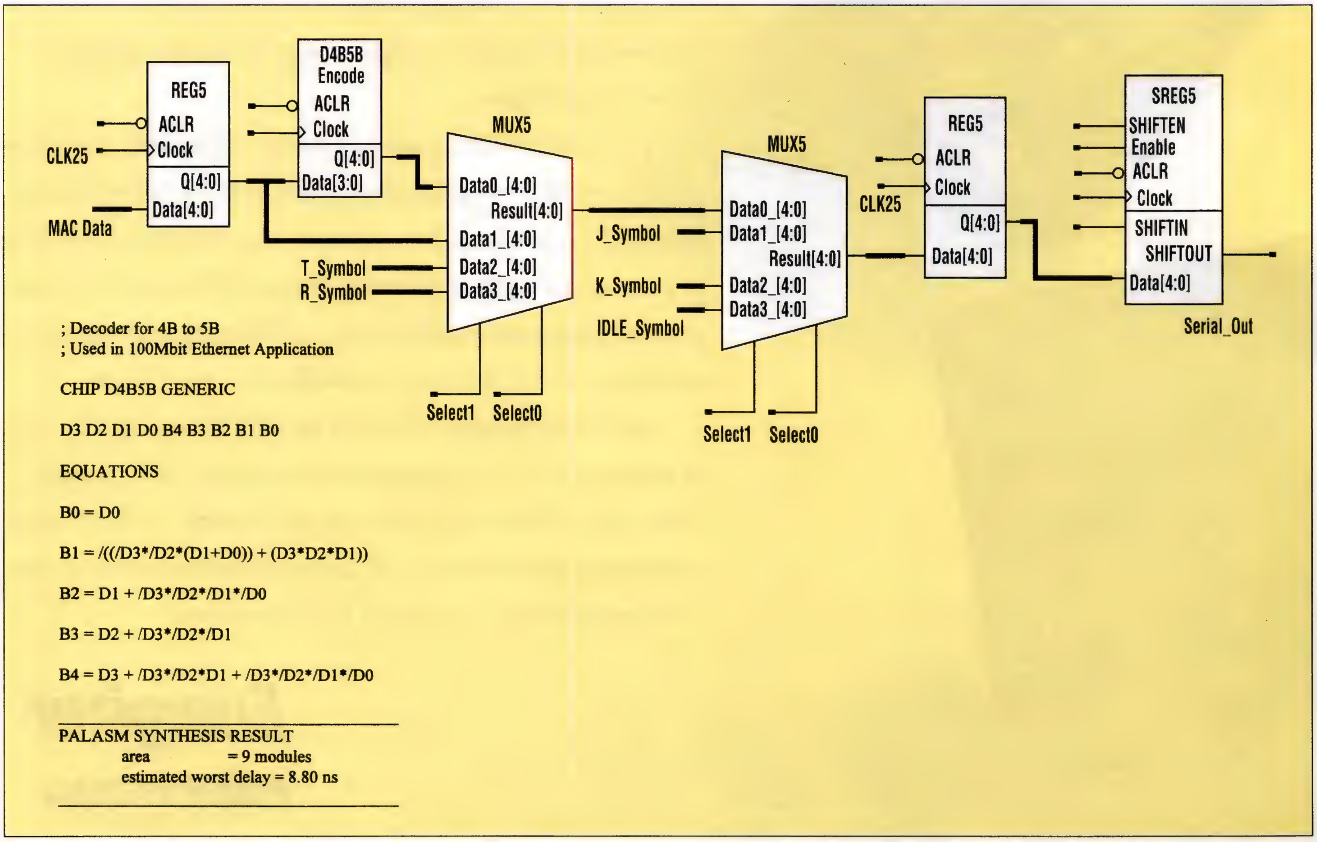
A squelch function filters out noise events by not allowing a transition to the Carrier state unless two non-consecutive zeros are detected. Because carrierSense is used by the MAC for deferral purposes, it must be asserted on the detection of any received signal (energy or non-Idle input), whether or not it's an actual packet. Because carrierSense also is used to detect collisions, it's important to avoid triggering on noise, specifically a single bit event. If Carrier is entered, RxDATA is initialized to all zeros (0000) and receiving is set to True.

The Align state is entered next. In Align, the process searches for the start-of-packet symbols /J/K/. If two Idle symbols (1111111111) are found instead, no start-of-packet was detected and the machine moves to the Idle state. If the /J/K/ symbols are successfully found, the Start state is entered. In Start, the MAC preamble data (55) is substituted for the received /J/K/. The waitQuint function assures that MAC data isn't overwritten.

Receive is the next state. In the Receive state, valid data usually will be received and a transition to the Data state will be taken. In the Data state, receiveError is deasserted and the 4B5B decoded data is sent to the MAC. From the Data state, the machine returns to the Receive state. If during the Receive state two Idle symbols are received, the Premature state is entered, receiveError is asserted, and Idle is reentered. If in the Receive state invalid data is received, the Data Error state is entered, receiveError is asserted, and Receive is reentered. Invalid data isn't transmitted to the MAC. If in the Receive state a /T/R/ symbol pair is detected, the End state is entered, receiving is deasserted, and Idle reentered.

Several of the receive-functions designs can be used to show some common techniques for high-speed FPGA applications. The entire design is too large to cover completely, but these selected functions illustrate the types of techniques used by FPGA designers in such classes of applications.

The shift and sync-detect block is responsible for shifting the serial data



```
; Decoder for 4B to 5B
; Used in 100Mbit Ethernet Application

CHIP D4B5B GENERIC

D3 D2 D1 D0 B4 B3 B2 B1 B0

EQUATIONS

B0 = D0

B1 = /((/D3*/D2*(D1+D0)) + (D3*D2*D1))

B2 = D1 + /D3*/D2*/D1*/D0

B3 = D2 + /D3*/D2*/D1

B4 = D3 + /D3*/D2*D1 + /D3*/D2*/D1*/D0

PALASM SYNTHESIS RESULT
        area                  = 9 modules
        estimated worst delay = 8.80 ns
```

3. THE LOGIC DIAGRAM FOR the transmit block shows that the main flow of data comes from the MAC at 25 MHz in a 4-bit-wide data word. The logic can be designed using the equations shown in the insert, which are automatically compiled with Actel's ActMap tool.

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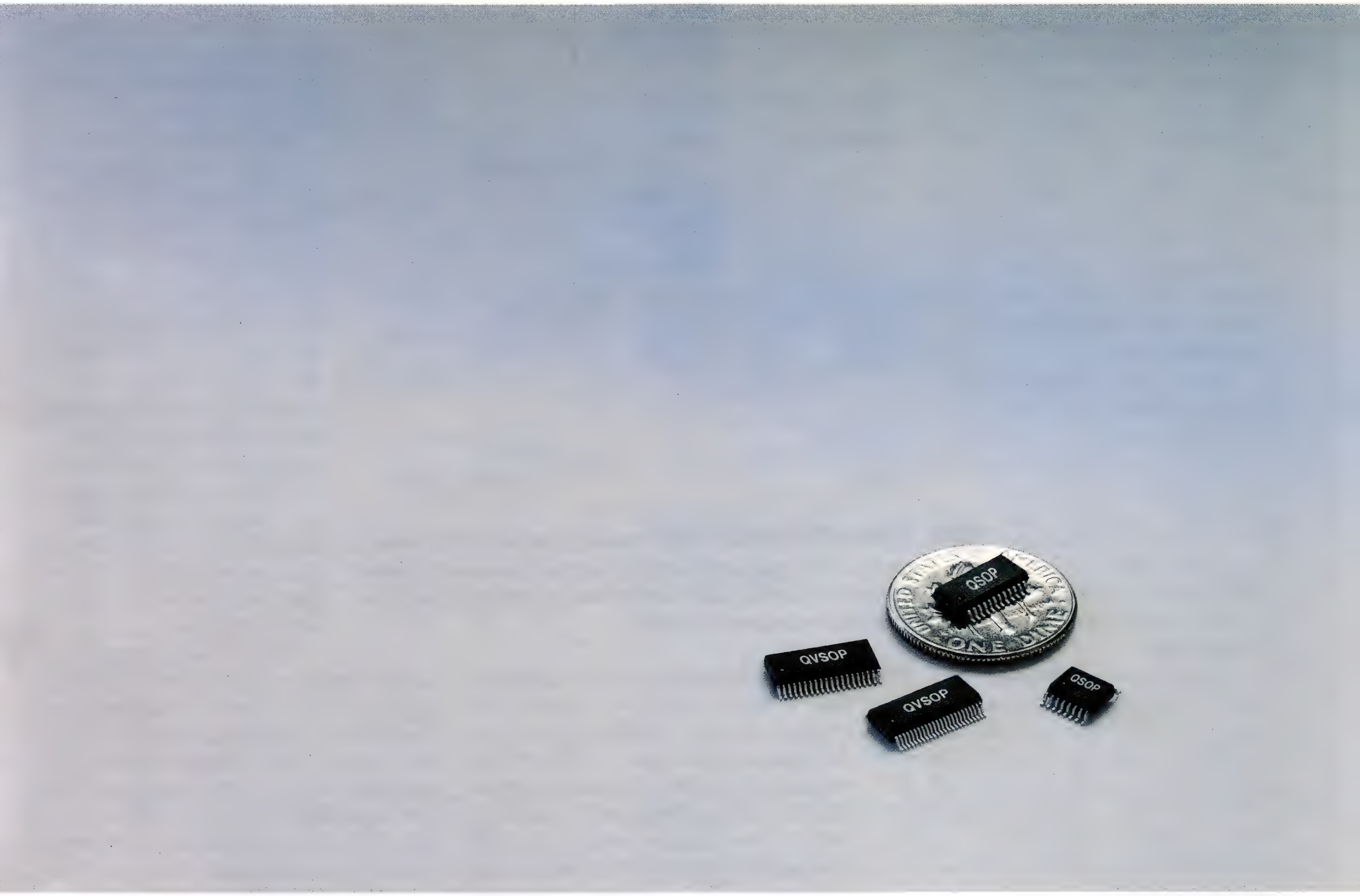

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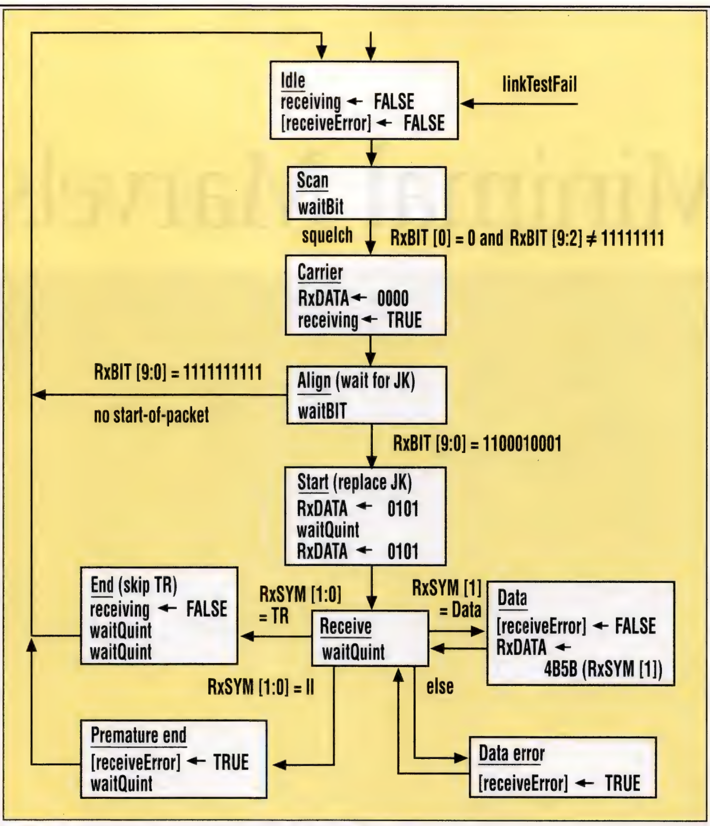
at the 125-MHz rate, and detecting the sync symbols *(Fig. 5a)*. Once a sync symbol is detected, the clock-generation state machine adjusts the 25-MHz symbol clock by stretching it the required number of 125-MHz clocks to align it with the symbol *(Fig. 5b)*. The symbol then can be captured by the 25-MHz clock correctly and decoded by the 4B5B decode block. The receive state machine tracks the received symbols to ensure a complete packet was received, and indicates the current line state to the protocol's next layer *(Fig. 5c)*.



4. TWO SEPARATE SETS of states exist in the receive state diagram. The Idle, Scan, Carrier, and Align states are pre-aligned and operate on the raw input bits using RxBIT. All other states are aligned and operate on the input data stream as symbols (RxSYM).

Serial data is clocked into the shift and sync-detect block using the 125-MHz clock. As data shifts, sync symbols are being detected. A single logic level, which is all that's required to detect the five important sync signals (J, K, T, R, and I), is detailed in the table.

Two of the shift-register bits (B3 and B4) have duplicated registers so that both the true and its complement are available. This is required to implement single-level decode for the I symbol, because the ACT3 logic module implements 5-input AND/NAND gates with at least two inverted inputs.

The technique of providing additional registers with inverted outputs is common when implementing logic functions using fine-grain antifuse FPGAs. The additional registers cost little because of the fine-grain logic module, and can be employed where needed to provide additional logic signals. The abundant routing resources available with antifuse FPGAs also supply the extra routing resources required to create such logic signals.

The squelch function filters out noise events. Zeros are ignored unless there are two noncontiguous zeros within the first ten bits. Initially, it would appear that the logic to detect two noncontiguous zeros in a 10-bit word would be quite extensive. However, once it's observed that this function is used only on a serial data stream, several simplifying logic reductions can be made. It will only be necessary to check the least significant bit (B0) and ensure that at least one of the higher order bits (B2 through B9, because B1 is contiguous) also is zero. This is necessary because any other combination is simply a shift from B0. The resulting logic equation:

S:= /B0 * (/B2 + /B3 + /B4 +
/B5 + /B6 + /B7 + /B8 + /B9)

is still too large to implement in a single logic level. Because the data is shifted in serially, the higher-order terms can be precomputed and then combined with the critical B0 signal using a single logic level. The resulting equation is:

S1:= /(/B1 + /B2 + /B3 + /B4)
S2:= /(/B5 + /B6 + /B7 + /B8)
S:= /B0 * (/S1 + /S2)

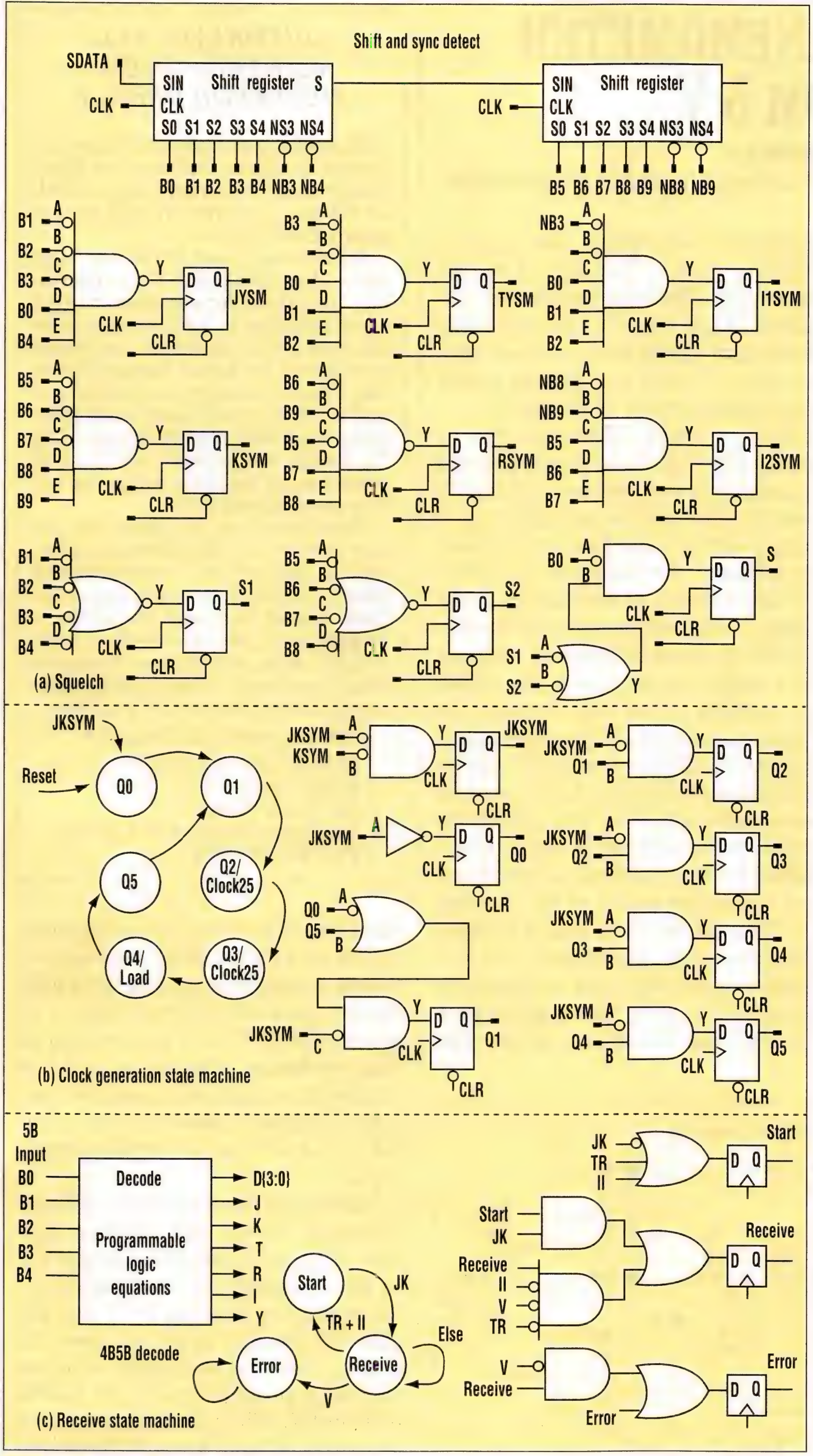
Notice that the B2-B9 bits in the first equation were replaced with B1-B8 in the second equation because of the additional level of registers (S1 and S2) placed between the incoming data and the output S. This form of pipelined operation works well in serial-data applications, and will almost always result in faster and area-efficient FPGAs.

Also, the extra inversions on the S1 and S2 terms are used because NOR functions with inverted inputs map easier into in a single ACT3 logic module. Synthesis software, such as Actel's ActMap Program, figures this out automatically, allowing the engineer to instead focus on architectural and functional issues. Thus, what initially looked like a difficult decoding problem can be significantly simplified to only three logic modules. The final design operates easily at the serial data rate.

The clock-generation state diagram divides the 125-MHz serial clock by five to generate the 25-MHz symbol clock, Clock25 *(Fig. 5b, again)*. The Clock25 signal is stretched when a sync symbol is detected to align it with the 5-bit symbols. This is accomplished by the transition to the Q0 state when the JK signal (start of packet) is active. Entry into Q0 synchronizes the 25-MHz clock (Clock25, the output from states Q2 and Q3) and the Load signal. The Load signal will be active every five clocks after synchronization to capture the 5-bit symbol from the aligned received data stream. The symbol then can be safely captured by the 25-MHz clock (Clock25) in the aligned symbol register (ASR).

Each state in the machine utilizes a single register. This one-hot state-machine-design technique uses the register-intensive nature of fine-grain antifuse-based FPGAs to reduce the logic to determine next-state transitions.

In traditional encoded designs, every state bit is needed to determine the machine's state, which makes



5. LOGIC DESIGN FOR THE receive block includes shift, sync detect, and squelch; clock generation; and 4B5B decode and receive. The shift and sync-detect block is responsible for shifting the serial data at the 125-MHz rate, and detecting the sync symbols (a). Once a sync symbol is detected, the clock-generation state machine adjusts the 25-MHz symbol clock by stretching it with enough 125-MHz clocks to align it with the symbol (b). The symbol then can be captured by the 25-MHz clock correctly, and decoded by the 4B5B decode block (c). The receive state machine tracks the received symbols to ensure a complete packet has been received, and indicates the current line state to the next layer of the protocol.

transition terms very complex and wide. FPGAs, on the other hand, can use the additional register available to reduce the logic complexity because only one register output is required to determine the state of the machine. Then the FPGAs' narrow, high-speed logic module can be used to generate the transition terms efficiently.

In fact, upon closer examination, the implementation of the state machine maps very closely to the state diagram. Transitions from one state to another result in a connection from the starting-states register to the entered-states register. Logic complexity can easily be estimated directly from the state diagram. Only one logic module is required to implement the most complex transition, so the entire machine runs easily at 125 MHz.

Once a symbol is aligned, the data must be extracted by converting the 5-bit input into the 4-bit data word. This conversion is done according to the 4B5B decode table. An implementation of the decoder in the ACT3 family is automatically generated by the equations developed from the encoding table. The full decode requires only 24 modules and two levels of logic, easily meeting the speed required for the 25-MHz clock.

The receive state machine in Figure 5 tracks the sequence of symbols received, and ensures that a complete packet is received without errors. The resulting state machine requires only four logic modules and two levels of logic. It reaches the required 25-MHz clock rate quite easily.

The receive and transmit blocks were designed and implemented in an Actel A1425A-2 device. The worst-case path in the 125-MHz section of the design was 6.6 ns, and the worst-case path in the 25-MHz section was 25 ns. The entire design required only 80% of a 2500-gate device. □

Warren Miller, a product planning manager at Actel and co-inventor of the industry-standard 22V10 programmable device, holds an MS in computer science from the University of California at Berkeley.

HOW VALUABLE?	CIRCLE
HIGHLY	527
MODERATELY	528
SLIGHTLY	529

CIRCLE **520**

LINEAR ANEMOMETER RUNS FROM 5 V

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290.

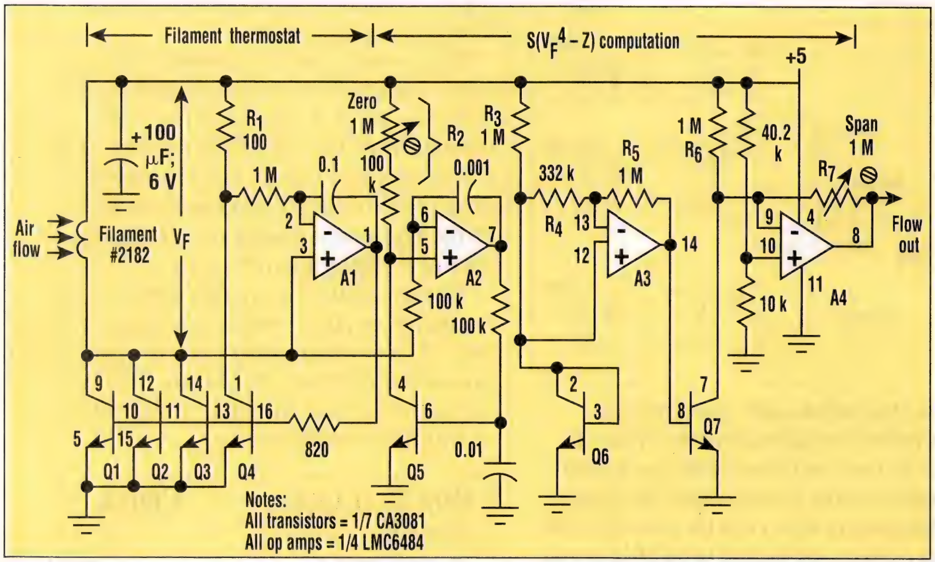
There are many ways to measure air speed, and the hot-wire anemometer is among the most popular. Using the predictable relationships of heat loss from a heated filament to air speed, and of electrical resistance to filament temperature, this technique provides a sensitive, no-moving-parts solution.

Most implementations of the hot-wire, however, suffer from two shortcomings. First, filament-temperature regulation is usually achieved by placing the filament in a bridge where filament current is measured by a sense resistor placed in series with it. Because the resistor's value is generally at least as large as the resistance of filament itself, half or more of the power applied to the bridge is lost in the sense resistors. This leads to excessive power dissipation and a requirement for power-supply voltages higher than 5 V.

The second shortcoming involves air speed. The air-speed measurement itself is proportional, not to filament voltage required to maintain a constant temperature, nor even to filament power, but rather to the *square* of filament power (the so-called "King's law"). Consequently, the output signal from hot-wire anemometer circuits is typically a very nonlinear function of air speed.

Both of these difficulties can be avoided by exploiting properties of a monolithic transistor array (CA3081) *(see the figure).* The squandering of supply voltage and power is avoided by utilizing the inherent transconductance match of transistors in the array, instead of passive series resistances, to control filament current. As a result, as A1 servos the collector current of Q4 and thereby the voltage across R_1, it simultaneously adjusts the filament (a 2182-type incandescent lamp denuded of its glass envelope) voltage V_F. The ratio of filament to R_1 current is stably maintained by the identical temperature and operating points of Q1 through Q4. The net result is that A1 drives the filament temperature to the value that causes filament resistance to equal $R_1/3 = 33\ \Omega$. This is about double the cold resistance of the filament and therefore, assuming tungsten wire with a 0.0045/degree coefficient of resistance, represents a filament operating temperature of around 230°C. This is hot enough so that moderate changes in ambient temperature are unimportant factors in filament power demand, but not so hot as to cause the filament to burn.

Rail-to-rail input amplifier A2 continuously servos the collector current of Q5 to V_F/R_2, making the V_{BE} of Q5 a logarithmic function of V_F. A3 multiplies this log by 4 and applies the product to Q7. Q7 does the antilog function so that its collector current is proportional to the fourth power of V_F. Thus, by King's law, it's proportional to air speed in the vicinity of the filament. This current is offset and scaled by A4 to produce a voltage output that, thanks to the rail-to-rail output capability of the LMC6484, can range from 0.01 to 4.99 V. Full-scale air speed can be adjusted, using R_7, to any value in the range of 1 to 10 meters/s.☐



Notes:
All transistors = 1/7 CA3081
All op amps = 1/4 LMC6484

THIS LINEAR ANEMOMETER, USED TO measure air speed, exploits the properties of a monolithic transistor array.

EDITORIAL CALL: WANTED—MORE IDEAS FOR DESIGN

We recently expanded the Ideas for Design section to include more items in each issue. To continue this expanded section, however, we will need a steady flow of ideas.

We depend on our readers to keep this section going. This is an opportunity for our reader-engineers to gain recognition for, as well as share, their innovative ideas with other engineers throughout the world. Issue after issue, Ideas for Design is voted highest on the "Of Interest" scale in our reader surveys. We pay $100 for each Idea for Design we publish, and the IFD voted best of the issue brings the author an additional $150.

Submissions to the Ideas for Design section should be about one typewritten page of text, with one or two circuit diagrams or block diagrams. They should represent the author's original work, be tested to prove they actually work, and not have been published previously. Please include telephone and fax numbers, if available.

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CIRCLE

521 SINGLE-SUPPLY PHOTODIODE AMP

JOHN A. HAASE
Colorado State University, Fort Collins, CO 80523; (303) 491-5545.

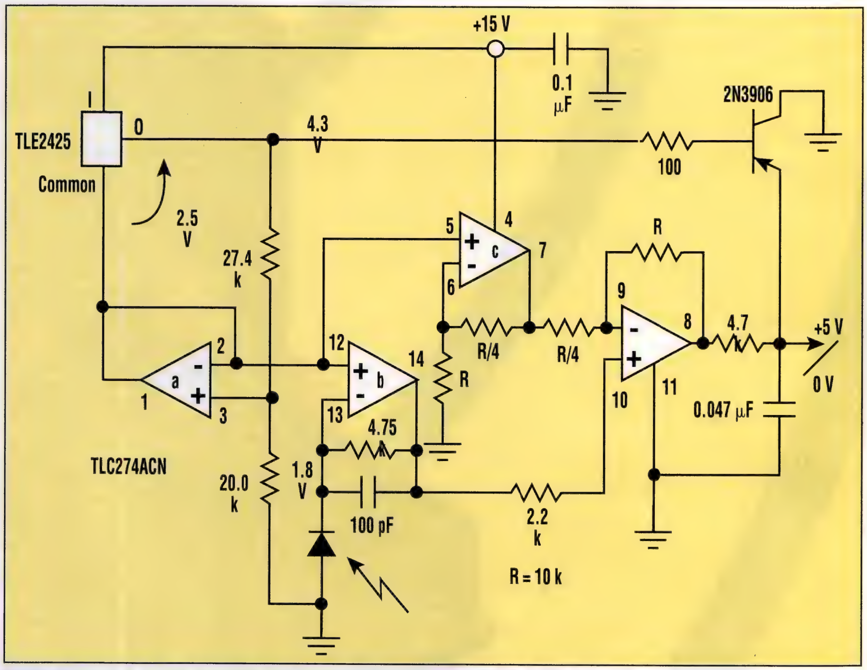
This circuit offers many features that are commonly required in circuits using photodetectors *(see the figure)*. For instance, it provides a reverse-bias operating point and output voltage offset, and uses a single-polarity power supply. On top of that, the circuit is designed to employ low-cost devices.

As shown in the schematic, the floating reference voltage from TLE2425 serves to bias the diode in a reverse-polarity mode. It also provides a clamping level at the output. Consequently, linear response to illumination is maintained for a 5-V range from dark current to full sunlight conditions.

Section b of the quad op amp is a current-to-voltage converter for photocurrent through the 4.75-k resistor. Bias voltage is fixed by the reference current (2.5 V/27.4 k) in the 20.0-k resistor.

Sections c and d of the quad op amp comprise a difference amplifier that has a gain that is set by the R, R/4 resistor pairs. These were chosen with pins 6 and 9 as the common node in a five-resistor SIP network. Four resistors can be paralleled simply by joining their terminals. The result is good matching and temperature tracking at low cost when both packages come from the same manufacturing batch.

The photodiode is a Hamamatsu G1115, which is intended for use in the visible spectrum.☐



THIS LOW-COST PHOTODIODE AMPLIFIER helps solve common problems associated with photodetectors, providing reverse bias operating point, output voltage offset, and a single polarity power supply.

IFD WINNER

IFD Winner for June 27, 1994

Marc Thompson, 19 Commonwealth Road, Watertwon, MA 02172. His idea: *"Low Voltage Offset Emitter Follower."*

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CIRCLE

522 TWO REMOTE METERS USE ONE WIRE PAIR

WAYNE SWARD
1648 Emerald Hills, Bountiful, UT 84010.

Driving two remote meters independently usually requires two wire pairs (one pair for each meter). However, this circuit drives two meters with only one wire pair, and its "constant current" design eliminates the effects of up to 200 Ω of wire-pair resistance *(see the figure)*.

In the circuit, IC1 and IC2 generate a 40-Hz symmetrical square wave (the frequency isn't critical). Q5 through Q8 amplify the square wave to 5 V p-p, which is applied to the "return" (black wire) for the remote meters.

Amplifier IC3A buffers the input signal voltage V_{M1}, intended for meter M1 (0 to 8 V), and sends it through emitter-follower Q3 to a 100-Ω current-sense resistor. The other end of this resistor is tied to the "supply" (red wire) of the remote meters. IC3B amplifies the voltage across the sense resistor, which corresponds to the current sent to remote meter M1, and closes the feedback loop to IC3A.

This results in a voltage of 0 to 8 V at the M1 input, generating a current of 0 to 10 mA to M1. Transistor Q1 gates this current on and off synchronous to the 40-Hz square wave, so that meter M1 actually sees a 50%

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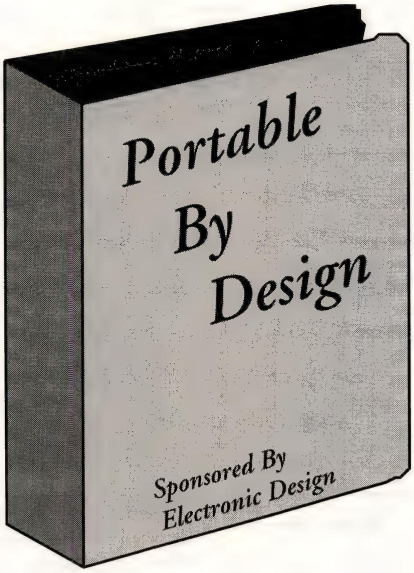

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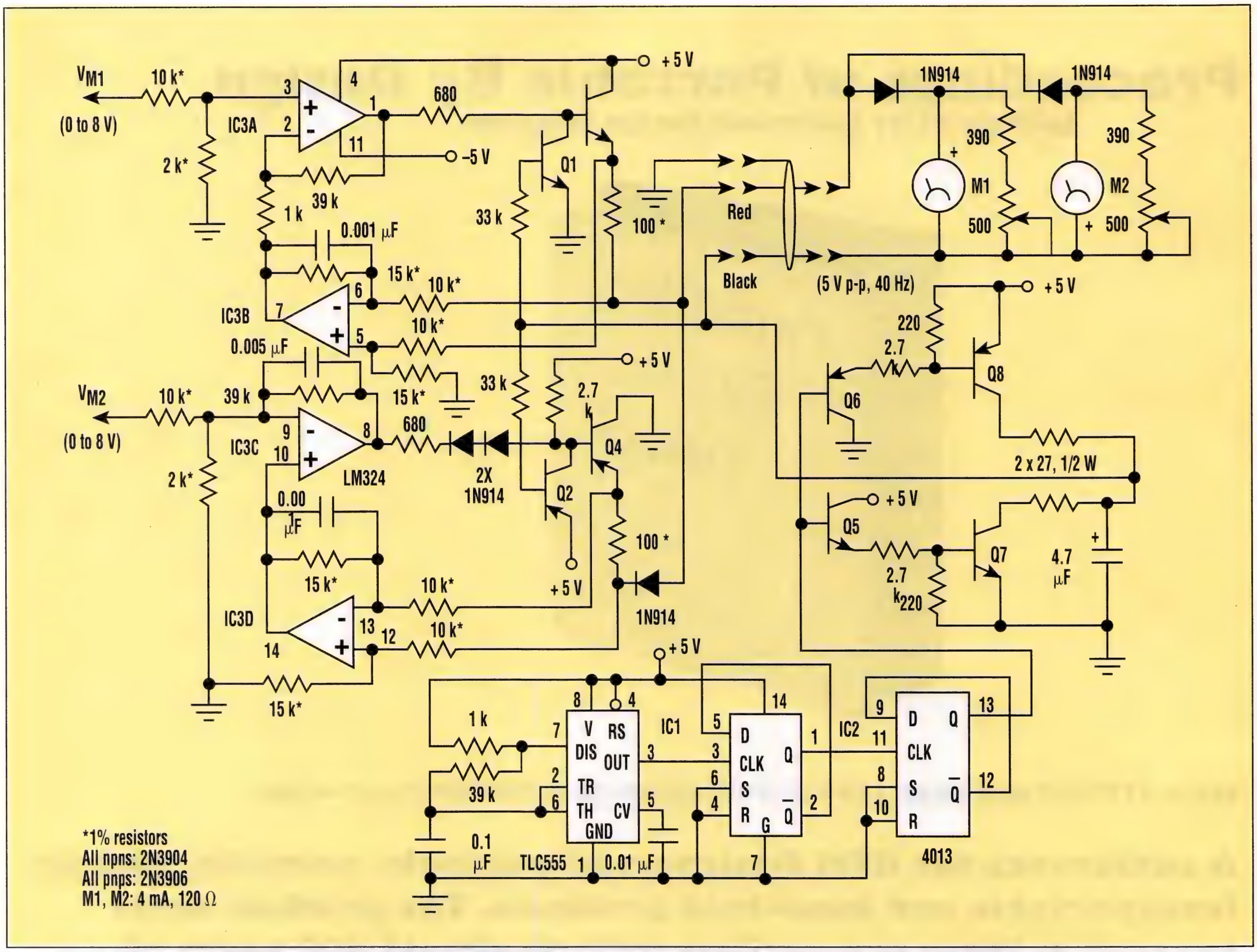

TWO REMOTE METERS CAN BE DRIVEN INDEPENDENTLY using just one wire pair. This "constant current" design eliminates the effects of wire-pair resistance up to 200 Ω.

0-to-+10-mA peak (0 to 5 mA average) current.

Similarly, IC3C, IC3D, Q2, and Q4 provide a 0 to –10-mA peak current for M2. M1 and M2 are isolated by the two reverse-connected 1N914 diodes in the remote-meter box. Variable resistors across M1 and M2 permit calibration. The extra 1N914 diode in the M2 drive circuit prevents interference between M1 and M2.

This particular circuit was installed in an AM/FM broadcast station, where it allows the studio operator to monitor the AM and FM transmitter modulations. The scheme is also suitable in a variety of monitoring applications.☐

Send in Your Ideas for Design

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CIRCLE 523

VARACTORLESS HF MODULATOR

MICHAEL A. WYATT and LARRY A. GEIS
Honeywell Inc., 13350 U.S. Hwy. 19 N, MS 931-4, Clearwater, FL 34624.

Traditionally, high-frequency oscillators are frequency-modulated by using a varactor as a voltage-controlled capacitance. Modulation is applied to the varactor in the form a voltage, which causes a capacitance change and subsequently alters the oscillator's frequency. However, varactors usually require a large voltage change to achieve a reasonable capacitance change--a problem in many battery-powered systems where supply voltages are limited.

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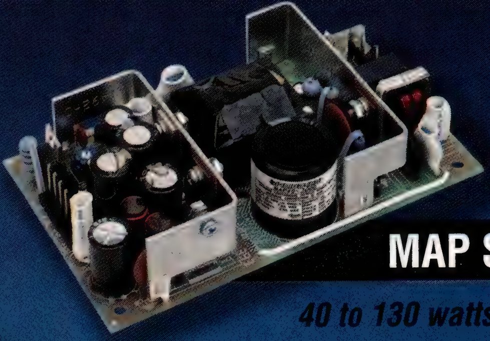

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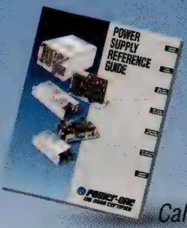

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tance modulation *(Fig. 1)*. The base-charging capacitance of a bipolar transistor is directly proportional to the collector bias current:

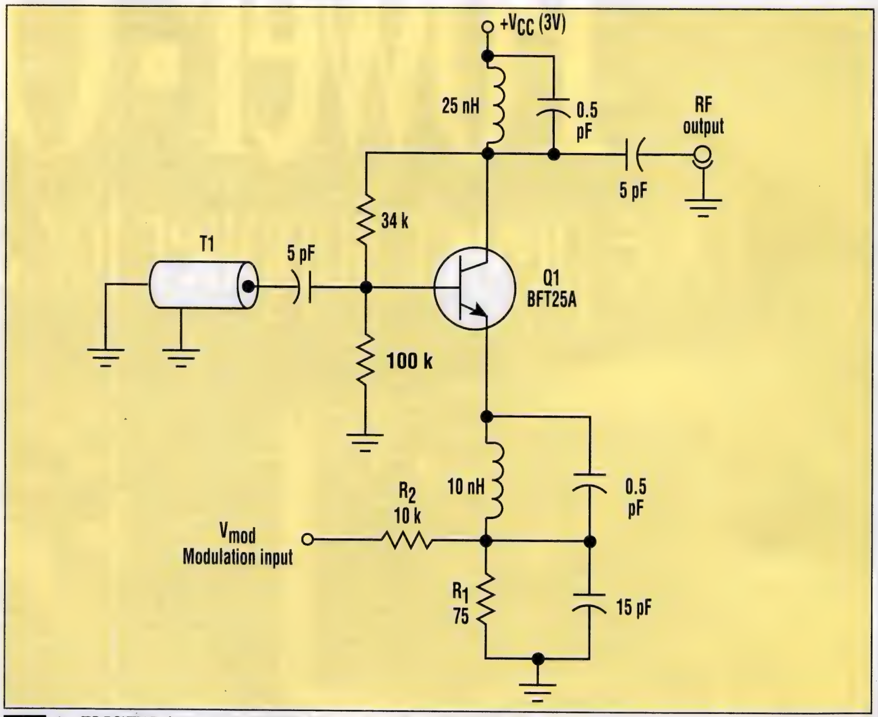
$$C_b = \lambda_F \times qI_C/kT$$

where C_b = charging capacitance; λ_F = base transit time; I_C = collector bias current; q = electron charge; k = Boltzmann's constant; and T = temperature in Kelvin.

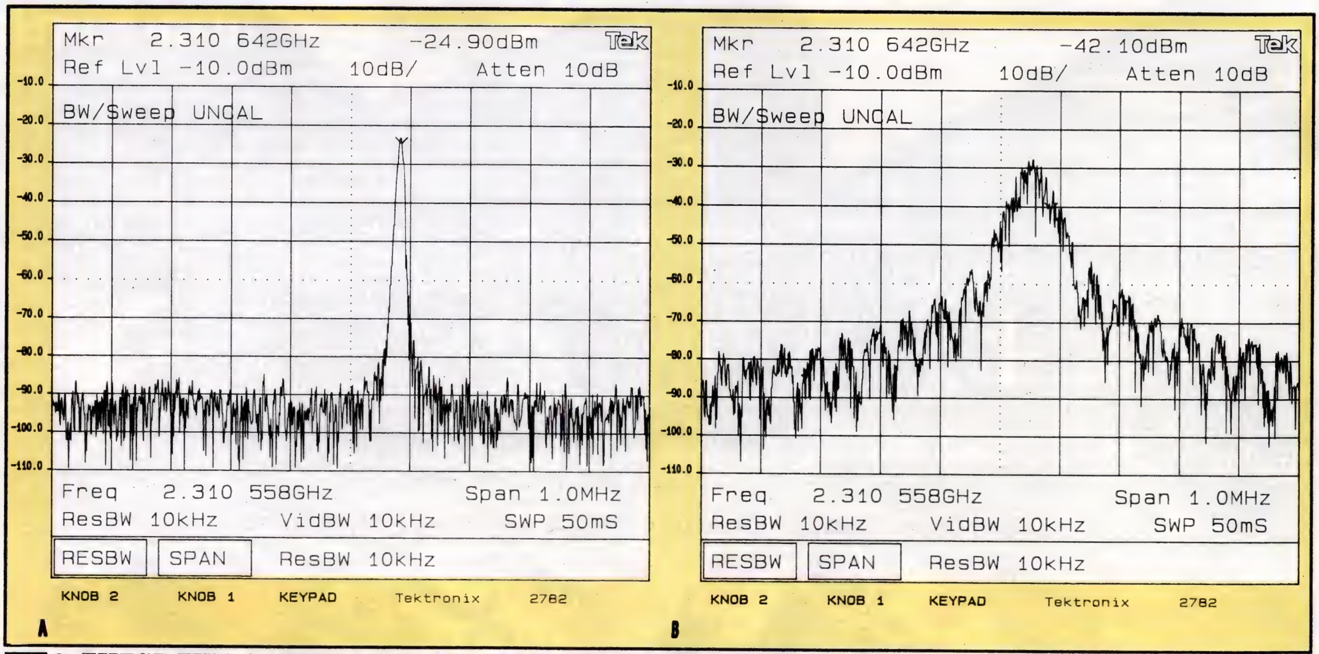
Resistor R_1 establishes Q1's current, while R_2 allows control of the collector bias current by V_{mod}. The transmission line (T1) in the negative resistance-type oscillator of Figure 1 determines the frequency of oscillation. T1 (Transtech 8800) is a high-quality, low-loss, ceramic coaxial shorted quarter-wave transmission line. Under proper terminal impedances, a negative resistance is "seen" at Q1's base. T1 reacts with this negative resistance to produce sustained oscillations *(Fig. 2a)*.

Frequency modulation is accomplished by changing Q1's collector bias current and thus changing Q1's base-charging capacitance. This effect is "seen" at Q1's base and causes a frequency shift in the resonate quarter-wave mode of T1. Figure 2b is a spectral plot of the oscillator with 100-kbit/s data modulation applied at V_{mod}.

The modulation produced from this circuit, if a digital data stream is used, is continuous-phase frequency-shift keying (CPFSK). By changing the amplitude of the data stream being injected into the oscillator, the frequency shift can be adjusted. In this example, the amplitude was set to produce a frequency shift necessary for minimum-shift keying (MSK). As can be seen in the spectral plot, a narrow power spectrum, often desirable in a crowded rf environment, is produced.☐



1. INSTEAD OF USING A VARACTOR to frequency-modulate a high-frequency oscillator, this concept employs base-charging capacitance modulation. Consequently, the large voltage change required by a varactor, which can be a major problem in battery-powered systems with limited supply voltages, is eliminated.

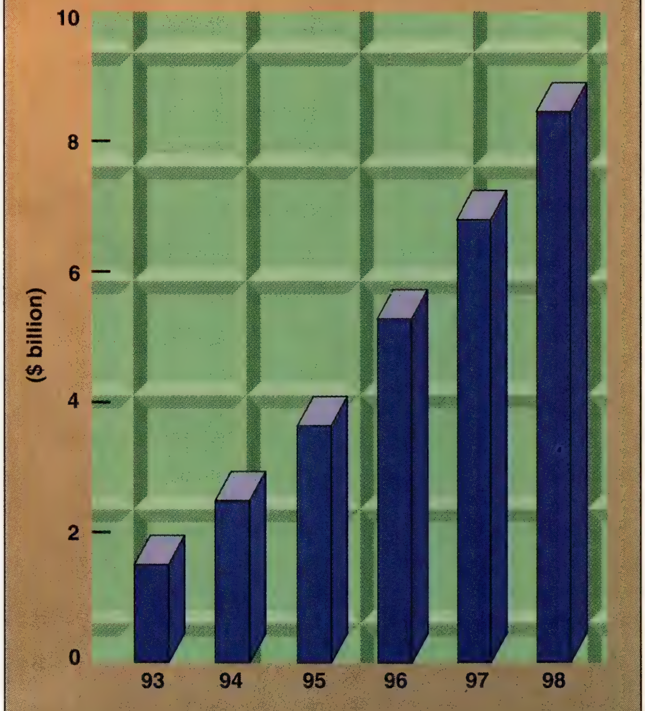


2. THESE TWO SPECTRAL PLOTS ILLUSTRATE THE sustained oscillations produced when transmission line T1 reacts with negative resistance (a), and the oscillator when 100-kbit/s data modulation is applied at V_{mod}.

ELECTRONIC DESIGN QUICKLOOK

EDITED BY SHERRIE VAN TYLE

MASSIVELY PARALLEL PROCESSING TECHNOLOGY SHOWS STRONG MARKET POTENTIAL



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MARKET FACTS

Massively parallel processing (MPP) computer technology is rapidly overcoming the hardware and software constraints that have kept it from widespread acceptance. A report from Electronic Trend Publications, *The MPP Computer Market*, describes barriers being hurdled and the healthy growth potential in the market for MPP technology. The San Jose, Calif., market researchers predicted that the market will grow at a compounded annual growth rate (CAGR) of 41.3% from $1.5 billion in 1993 to reach $8.4 billion in 1998.

Technical advances include efforts to standardize Unix for multiprocessors and the development of new parallel-processing languages such as Sisal, Occam, Super, KRC, Miranda, and parallel versions of C and Fortran. Hardware advances include the use of off-the-shelf microprocessors and the increasing popularity of virtual shared memory.

EYE ON ISO 9000

When the International Standards Organization (ISO) first breathed life into the 9000 series in 1987, 3M supported the committee's efforts with enthusiasm. Today, more than half of all 3M U. S. sites have earned registration, with all European 3M sites registered. Compare this with the fact that less than 1% of all U.S. manufacturing sites are currently ISO registered.

So, was the effort really worth it? Is 3M, a leader in the ISO 9000 movement, truly reaping the benefits of registration? Definitely. Certification is very important to us. ISO 9000 is assurance to our customers that 3M has quality systems in place. In addition, after we certify confidence in our key suppliers, we do not have to monitor and inspect all shipments. This effectively removes non-value-added costs out of the system.

Registration has brought many other benefits, including:

- Reduced production costs: The procedures reduced the need for rework.
- Competitive advantage: ISO 9000 is an important marketing tool for promoting company products and services.
- Focus on quality-management systems: We measure and improve internal quality procedures at all levels of the company, as opposed to strictly evaluating product specifications and performance.
- Global marketing opportunities: Since standardization is being emphasized in Europe, ISO 9000 may be a prerequisite to entering new international markets.
- Workplace unity: ISO 9000 provides a common focus for workers, creating the groundwork for improving teams.
- Product quality: Customers consistently receive high-quality goods.
- Customer cost savings—no need for costly supplier quality audits.
- Common language for communication: Customer and supplier have common guidelines and language for communication about product specifications, quality level, and other criteria.

The many benefits of registration do come at a price. Cost is a major stumbling block for many organizations that lack resources for this intensive process. And there's inconvenience: Once management makes the commitment to pursue ISO registration, you must get the entire organization to buy into the concept. This involves educating the workforce, organizing and documenting your programs, and maintaining plant operations to ISO specifications.

By Thomas Niccum, Division Vice President, 3M Electronic Products Div., Austin, Texas.

QUICKLOOK

QUICK NEWS: AWARDS

The 1995 DuPont Plunkett Awards for innovation with Teflon recognize companies and developers contributing new products and/or applications. To be eligible, new or improved products must use DuPont Teflon fluoropolymer resin or Tefzel fluoropolymer resin. The program is conducted worldwide, with regional awards from the Americas, Europe, and Asia. Each entry will compete for a prize in electrical/electronic; chemical processing; and all other uses. One of the three category prizewinners will also be selected as best overall. Products or applications must have been put into commercial service in the marketplace between June 17, 1989 and June 16, 1994. Overall judging criteria will focus on innovation, breadth of application, and signficance/impact. Entries for each category will be judged separately, with one winner in each category. The deadline for entries is December 16, 1994. Each winning entrant will receive a commemorative sculpture and each winner's company will receive a $5000 cash prize. Grand prize is a special sculpture and an additional $2500 cash prize, to be divided equally among the entrants responsible for the grand prize-winning entry. Winners will be selected by experts from plastics industries, industry associations, the press, and academia. For entry forms or more information, contact Plunkett Awards, Hanes-Lahr Public Relations, 400 N. Capitol St. NW, Suite 550, Washington, DC 20001; (302) 999-2413.

QUICK REVIEWS

With 300 articles new to this edition, *The McGraw-Hill Encyclopedia of Science and Technology* gives information on new developments in 75 disciplines, including bioelectronics, fiber-optics imaging, cosmogenic nuclides, and superstring theory. The encyclopedia's 7900 articles cover the important aspects of physics, earth science, acoustics, chemistry, and computers. The volume is cross-referenced, with more than 1600 photographs and line drawings, plus tables, charts, diagrams and graphs. Appendixes cover mathematical notation, the International System (SI), the periodic table of the elements, and fundamental constants. The 2241-page book lists for $115.50 (ISBN: 0-07-045560-0). The book may be ordered by phone: (800) 262-4729. For further information, contact McGraw-Hill Inc., Professional Book Group, 11 West 19th St., New York, NY 10011; (212) 337-5945.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Let's continue exploring the components—time to market and break-even after release—that contribute to break-even time. From a common perspective, we now know marketing effectiveness, sales performance, manufacturing competitiveness, and distribution efficiency contributes to the production of the break-even after release (BEAR) metric. Measurement of break-even after release shows how fast you can ramp profit dollars—the more money that can be made in the shortest time the better. But a major part of the business equation, investment, remains hidden. Measuring time to market shines the light on new product investment.

I'm now advising three start-up business ventures. The size of the companies varies, but they share one strong common bond—money. They only have so much of it on hand, getting more takes a lot of work, and doing the right things with it separates the winners from the losers. And as you might expect, determining with high accuracy when the first product gets to market dominates much of the work we're doing because time to market and the management of investment money go together. Engineers look at the work they must perform and estimate the number of person-months they consume doing it. Likewise marketing and manufacturing do the same and determine their total person-months of effort. Knowing person-months gives us the information needed to staff for time. Of course, the product's basic definition forms the foundation for all this work.

With a working product definition, a cross-functional work structure, and staffing needs identified, we have most of the information needed to compute investment cash-flow profiles. On the basis of technology, customer, market, and staff information, we produce uncertainty figures that modify work content upward. As work content grows, total development cost increases. We then have control of when the product enters the market by the functionality we assign to full development and the staff levels we apply to do the work. From this structure, we produce time-to-market and new-product-investment figures. And when we are done, we have two, and more if we want them, trails through investment time we can use to track against—an investment cash flow profile and an investment staffing profile.

As these new businesses compare actual money spent and actual staff levels to forecast, they learn about their time-to-market performance. Actuals tracking close to forecast means: (1) the product definition allowed for cross-functional, concurrent development with minimal complication and delay; (2) the money and staff applied to the effort performed effectively; and (3) the organization broke out of the cerebral definition phase and actually did cross-functional, concurrent engineering. I see these three primary indicators by looking at time-to-market information. Note that TTM provides no indication of market success—BEAR does that. TTM does, however, provide an integrated metric to observe product definition stability, development cost, and development time.

A key point resides in the previous paragraphs—a single number does not constitute a time-to-market indicator. To make the time-to-market metric work, you'll need do trend analysis from the beginning to the end of the investment period. As a minimum, set a cash flow reference through time and a staffing profile reference through time. Next compare actual occurrence to the forecasts. Based on what you see, take the actions necessary to get back on track and meet overall time-to-market objectives.

Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.

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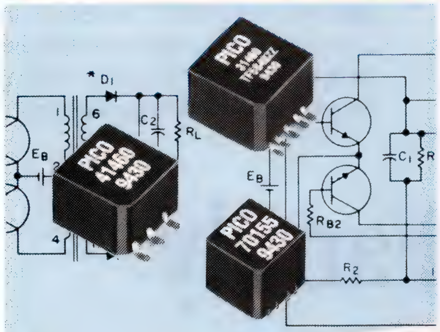

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...Vaarrooom! Doing 60

BY FRANK J. BURGE
Director of Market Development for Electronic Design

Seven weeks ago my chronometer clicked past 59, and there I was, 60. Holy smokes, how time does fly when you're having fun. It seems like yesterday that I was the youngest engineer in the group at IBM, Kingston. We worked on the AN/FSQ-7 computer, which was built with vacuum tubes. In 1960 I turned in my slide rule for a salesman's bag at the Systems Division of Beckman Instruments. I sold PDP-1 based data-acquisition systems and again was the youngest player on the team.

The PDP-1 was Digital's first computer. As I recall, a total of 53 were sold; Beckman bought 25, which made us a major customer. Today, if you buy 25 computers, you're nobody's biggest customer—unless the computers are of the supercomputer variety. Times do change.

Reaching 60 is a milestone of sorts, at least that's what my buddy Gus tells me. Gus and I grew up together on the southwest side of Chicago. After we went to grammar and high school together, I went off to study engineering; he went in search of a basketball scholarship. After laboring on the hard court for four years, he was able to get his medical school financed by the Veteran's Administration in return for a four-year tour in a VA Hospital. When Gus turned 60 last May, he retired from the radiology game in Peoria for what he had hoped would be a career as an organic farmer in Southern Illinois. But when I talked to him a few weeks ago, he's decided to go back to school and study computer science. Now he plans to start a software company: Windows for Hypochondriacs. Gus and my barber have one thing in common—they're both smart cookies.

The upside of being 60 is that over the years one has the opportunity to build special relationships. Relationships with guys I've known since I was in knickers and women who I went to grammar school with. And a very special relationship with my roommate, who I met 40 years ago in a saloon on 59th and Western in Chicago. My buddy Carney and I had gone there to have a few beers and see if we could meet girls. When I saw her sitting there with her five girlfriends, I figured it would be a miracle if she ever danced with me.

So I threw a quarter in the jukebox and played Glen Miller's "In the Mood" three times and then asked for a dance. Fortunately, she said yes or else it would have been a quarter down the tubes. And since it was Carney's quarter, he would have been miffed. While we were jitterbugging to the third round of Miller, I noticed she was making faces at her friends to let them know I was nutso. Seventeen months later we were married in one of the worst snowstorms ever to hit Chicago. Carney agreed to be in the wedding party if he got his two bits back. What a grand day it was.

So what does any of this have to do with the electronics business, system design, time to market, coping with technology racing by at blazing speed, or building a competitive advantage in the nanosecond nineties? Or surviving downsizing blitzes that will last till the end of the century? The fact is it has everything to do with it, because before long everyone will do 60. And while you're doing 20 or 30 or 40 or whatever, be sure you're not too busy building a career or too caught up in the demands of the fast lane to nurture the relationships that will last longer and mean more than anything you've ever done, more than anything you could dream of doing. Vaarrooom! Put a dollar in the machine, turn up the volume, listen to those trombones—Glen Miller lives. Nutso indeed.

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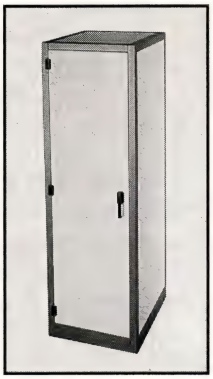

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PEASE PORRIDGE

WHAT'S ALL THIS FLIP-FLOP STUFF, ANYHOW?

A few months ago, I read that a new philosophy called "The Laws of Form" could help you design a D flip-flop with a smaller number of gates.[1] THAT reminded me of a trip I took 20 years ago, during which I actually did design a D flip-flop myself. I was working with some guys at Amelco, in Mountain View, Calif., on the industry's first 12-bit ADC IC, and I wanted to make a small, compact D flip-flop. I tried to do a design on the west-bound plane, but my efforts were utterly useless. I looked at the Design Rules, and I could not *begin* to design a layout for a D flip-flop. I did not know how to start.

BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Then when I got to see our collaborators, I took a look at *their* layout. OHHH, that's what a flip-flop layout looks like. I studied their design and took a copy back to my motel room. That night, after I comprehended their good layout, I designed a *better* layout that was not only 12% smaller, but 20% faster. We "analog" guys get the privilege of studying other peoples' best efforts, and if we can improve on them, we're considered wise. In this case, my cell was smaller and narrower, so a cascade of 12 of them would be a more compact block. Also, the delay to the Q-bar output was worse, but the delay to the Q output was smaller, so the ripple counter would have less delay during a ripple carry such as from (0111 1111 1111) to (1000 0000 0000).

The next day, when the Amelco guys looked at my best layout, they figured out a way to improve my layout by another 3% decrease in cell area. I then looked at their latest effort, and conceded that I could make no more improvement.

We built the circuit, and it worked the first time. We got it into production in 1975, and we sold some. (Note, all previous converters of this much resolution were designed to be digital voltmeters, putting out their drive to LED segments. This was the first one designed to interface with 12 lines to do a straight 12-bit binary output, coded as an ADC.)

I haven't done much design on flip-flops since that time, but the world doesn't need me to design flip-flops. I heard somewhere that there are 10,000 different designs for a 2-input NOR gate, each one *slightly* different. With that many gates, who needs me?

When I found out that you could use "The Laws of Form" to make a "better" flip-flop, I got curious. Could you *really* do better than the best efforts of designers over the last 30 years? Oh, yes, "The Laws of Form" showed how you could make a T flip-flop (divide-by-2 circuit) with only six gates, instead of the usual nine. WELL, that sounded like a little progress. BUT, since the guy who drew this to my attention made some "fuzzy" comments, I was prepared to be skeptical. Skeptical? Who, me?

I studied the proposed design for the "new, improved" flip-flop. Yes, there were only six gates—but each gate was a 3-input gate. Now, a CMOS inverter needs only two transistors, and can respond fairly fast. But a CMOS 3-input gate requires you to use six transistors, so it's definitely not as fast. In fact, a flip-flop that needs six 3-input gates will be much *larger* and *slower* than a conventional one that needs nine 2-transistor gates.

NOW, I'm in favor of trying out new concepts. If a novel approach really gives better results overall, hey, that's great. But if a new scheme merely has fewer gates, but more transistors, more area, and slower response, I can't get very enthusiastic. Further, as a friend pointed out, that 6-gate flip-flop isn't really new, since TI published that circuit more than 10 years ago. And it has few gates, which makes it hard to test....

If you want to build a flip-flop using just six transistors, as one engineer claims to have done, well, yes, you can do that, but it won't have the low-power advantages of CMOS. That sounds like RTL (resistor-transistor logic) to me, and hardly anybody uses RTL these days. The resistors get too bulky. It's transistors that are cheap, and resistors that are bulky and expensive.

George Spencer-Brown, the developer of the Laws of Form, is quoted as saying that when he began working as an engineer, he "realized the tools with which engineers worked were totally inadequate."

Spencer-Brown continues, "I gave a talk recently to engineers at Bell Labs ... but ... some time after my talk, they came to me and showed me a circuit they had designed using my principles, but it had three times the number of transistors that it needed. It seems I am the only engineer who can do it properly."[2] Yeah, everybody's out of step with Johnny.

The Laws of Form claim to introduce "imaginary logical values" for circuits with feedback. "Armed with these imaginary values, digital engineers can now analyze circuits with equations, rather than antiquated state diagrams."[3] Sounds like jolly fun for somebody else—for academics who have to publish and never have to

PEASE PORRIDGE

make things that work. For example, the standard definition of m to the n power is m times itself n times. "This is not only wrong, but it makes us think that taking something to the zeroth power is some kind of mystery," says Spencer-Brown.[4] Well, what's wrong for you may be right for me. I sure hope so.

I sent away for the book, *The Laws of Form*,[5] just to satisfy my curiosity. Maybe it could help me design a better op amp. But when I got it, I found that it has nothing directly related to electronics, or ICs. It shows the philosophy of a certain type of abstract symbolic logic. The book is crammed full of statements such as:

"Distinction is perfect continence." "There can be no distinction without motive, and there can be no motive unless contents are seen to differ in value." "The form of any finite cardinal number of crosses can be taken as the form of an expression." "*Knowledge*: Let a state distinguished by the distinction be marked with a mark ⏋ of distinction. Let the state be known by the mark. Call the state the marked state." "*Form*: Call the space cloven by any distinction, together with the entire content of the space, the form of the distinction. Call the form of the first distinction the form." "*Value*: Call a state indicated by an expression the value of the expression." "*Equivalence*: Call expressions of the same value equivalent. Let a sign = of equivalence be written between equivalent expressions. Now, by axiom 1, ⏋ ⏋ = ⏋. Call this the form of condensation...."[6]

If you like these, then you'll have a lot of fun. And if you want to learn how to make a better flip-flop—well, maybe this book will tell you how to do it. Good luck.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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References:

1. *E.E. Times*, CMP Publications Inc., 600 Community Dr., Manhasset, NY 11030. Feb. 14, 1994, pp. 1, 31-35; Feb. 21, pp. 31-33.; March 7, pp. 43, 62; March 14, pp. 37-39.
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5. *The Laws of Form*, by George Spencer Brown, Tarati Press, Published by Cognizers Connection, 4th Printing, 1994. Order from Bookmasters, (800) 247-6553 or (419) 281-1802; fax (419) 281-6883. About $50.00, plus $5.00 S&H
6. Ibid., pp. 1-16.

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A SPECIAL EDITORIAL FEATURE

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ELECTRONIC DESIGN

Designing With Surface-Mount Switches

The demand for downsizing and processing concerns make for plentiful design decisions.

BY LYLE FETTE AND TOM GEHRMAN

Mepcopal Co., 11468 Sorrento Valley Rd., San Diego, CA 92121; (619) 481-0210.

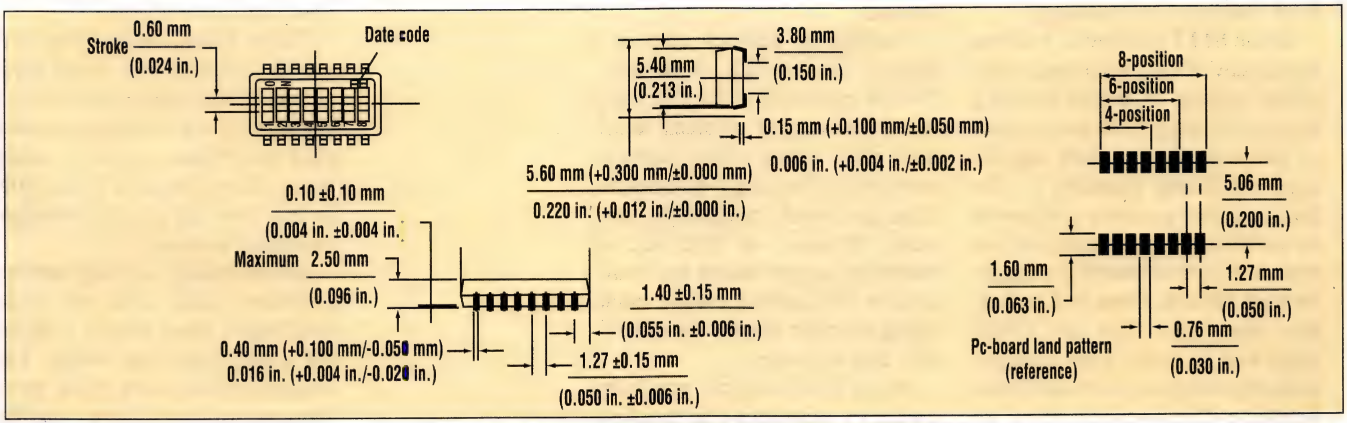
The latest generation of miniature, surface-mount switches offers circuit designers the opportunity to create more compact designs. What results is better use of board real estate, a reduction in end-product size, higher manufacturing yields, and lower installed costs. However, surface-mount technology (SMT) has its own design tricks and parameters, and the engineer must be aware of them. This article will examine some of the issues to consider when designing with surface-mount switches.

Downsizing, or saving board space, is a prime consideration in every designer's mind. However, developments in miniaturization techniques have made this goal simpler to attain. Comparing a traditional leaded product, which typically has a 0.100-in. lead pitch, with its latest surface-mount counterpart with 0.050- or 0.025-in. centers, clearly shows that from a board-layout standpoint, an SMT component can occupy less than half of the real estate.

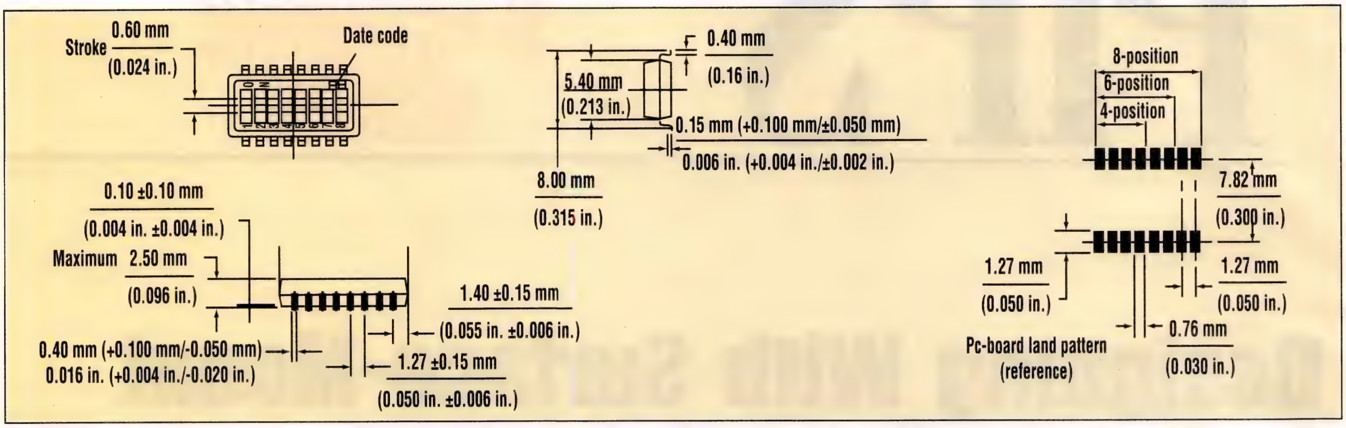
SMT-switch options include J-leads and the gullwing configuration. In the J-lead style, the pins bend underneath the part, saving additional board space *(Fig. 1)*. In the gullwing configuration, the leads bend away from the part *(Fig. 2)*. But the choice of lead style doesn't solely hinge on real-estate considerations. Engineers tend to favor one or the other based largely on what they have used previously.

J-leads take up slightly less board space, but the solder joints are underneath the part and can't be seen. A surface-mount part with gullwing leads takes up a bit more board space, but the solder joints are visible. The design consideration is whether there's a need to visually inspect the solder joints or do testing on the part. If either of these is the case, then the designer should consider gullwing over J-lead configuration, particularly since it provides a place for test probes.

Testing and probing become an issue when the customer has an expensive, high-density board with a large number of components. When one must put the board on an automatic circuit tester and come up with a fault warning isolated to a specific area, then design engineers require easily accessible probe sites on the circuits to determine



1. In the J-lead style for DIP switches, the pins bend underneath the part, saving additional board space. The downside, however, is that the solder joints are underneath the part and can't be seen for inspection.



2. In the gullwing configuration, the leads of a DIP switch bend away from the part. The leads take up a bit more board space than do those of a J-leaded design, but the solder joints are visible. The design consideration is whether there's a need to visually inspect the solder joints or do testing on the part.

exactly which component, and which lead, is the culprit. In this situation, the trade-off of exposed leads for more board real estate pays off.

At the other extreme is a case in which the designer tries to shrink an inexpensive board by 50%. There, the J-lead style is the obvious choice because real estate is the main concern. If some component fails, the board can simply be discarded instead of trying to repair it.

There are other reasons for choosing one lead style over another. For example, a slide switch may have six to eight positions that are actuated frequently. Because engineers don't always have control over how carefully the part will be handled, they may be concerned about the solder joints during the switching process. The gullwing style lends itself to visual inspection of the solder joints, therefore it may be prudent to use a gullwing-leaded switch so that the joints can be inspected more easily for solder-joint fractures or cracking.

Some SMT products, such as toggle and rocker switches, have either plastic or metal locating lugs protruding from the bottom of the component that can be used as fixing locators in the board. Their primary purpose is to stabilize the component so that as a user actuates the toggle or slide switch, there will be further assurance that the solder joint won't break. This configuration provides extra robustness because the locator tabs go through the board.

From a design standpoint, there are positive and negative aspects to using fixing locators. If a customer wants a true "vanilla" SMT board, there will be no joy over the prospect of either drilling holes in them or having them fabricated with locating holes. But such trade-offs are part of the designers' lot. If you must use a switch requiring considerable end-user actuation, it may be wise to consider those locating devices.

Many of the older SMT switch products still available are on a 0.100-in. terminal lead spacing. Newer products typically have 0.050-in. lead spacing for two reasons. The first involves size considerations. But the second, and more important reason, is that a 0.050-in. and even 0.025-in. size is compatible with the typical board layout in which ICs and other devices are surface-mounted *(Fig. 3)*. Switch packaging takes its cues from the layouts required for the commonly used ICs and discrete devices.

Packaging choices also is a factor in switch selection. Switch products offer the same three packaging choices available with many other surface-mount-technology products: tape-and-reel, magazine, and bulk. Because of the size of switches, no products are available in the cartridge-type packaging used for many chip capacitors and resistors.

Most DIP-switch products come in tape-and-reel packaging. Some of the larger products, such as toggle switches, rocker switches, and some of the miniature rotary switches are provided in magazine packs. Although miniaturized versions of these products are sometimes available in tape-and-reel, the magazine pack is the common configuration for larger switches.

Due to the nature of switches, switch manufacturers haven't been confronted with all of the electrostatic-discharge (ESD) requirements and problems associated with active components and some capacitors. However, in efforts to make their packaging specifications more uniform, increasing numbers of manufacturers are establishing ESD requirements. This is being driven by large multinational OEMs, many of whom require that even non-ESD-sensitive switches conform to ESD packaging requirements. The preference is to have one general packaging specification for all products, and most of these general specifications require electrostatic-discharge protection.

Tape sizes, including tape width, could profit from additional standardization. Most of these tapes are used in automatic pick-and-place assembly equipment. However, this technology is too new for an all-pervading standard to exist.

Occasionally, an engineer encounters parts that are wider and larger than others and call for a different tape width. This sometimes occurs with parts from suppliers in Japan and Eu-

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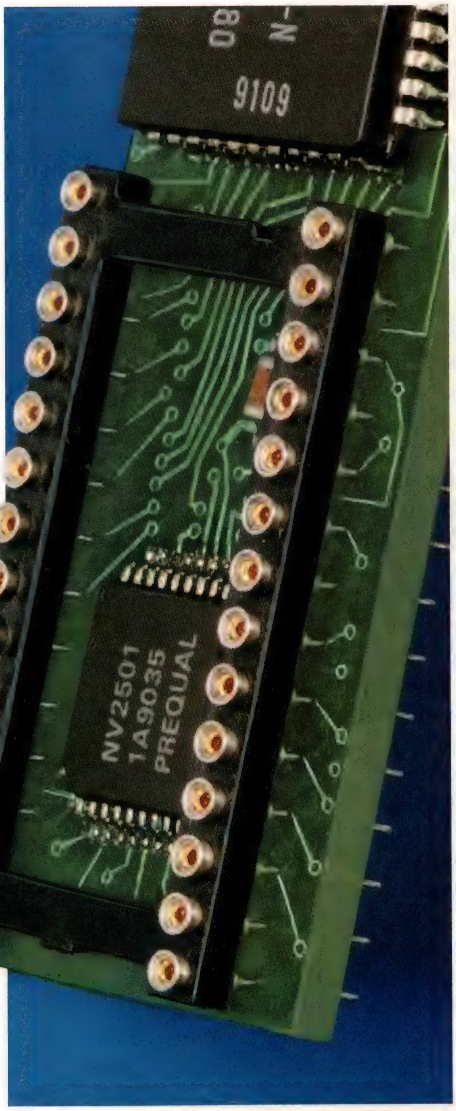

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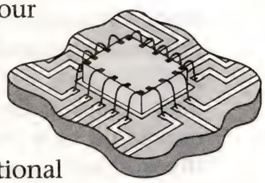

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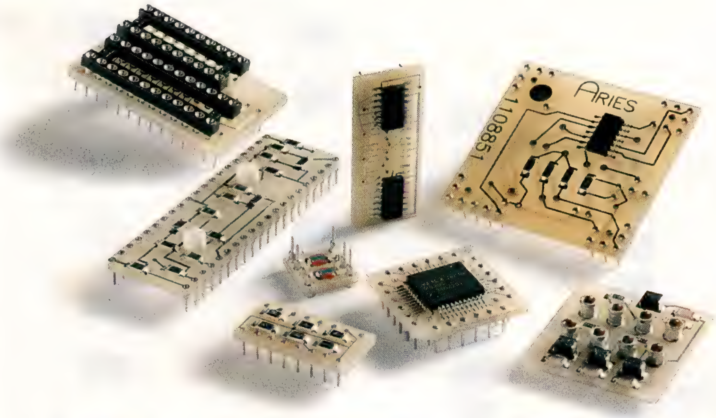

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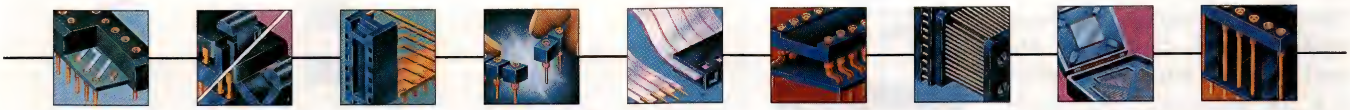


Sensible Solutions. . . Fast!

rope. Engineers must be aware of the tape widths their suppliers are using. If tape-and-reel packaging is being considered, it's necessary to ensure that the suppliers' tapes conform with either EIA or ANSI standards. Otherwise, non-conformance may come to light at the worst possible moment—when trying to run a given part through placement equipment.

Processing is another important consideration for designers. One of the more common problems with SMT processing is that, usually, some sort of a vacuum pickup is used for SMT parts. Hence, there must be an awareness of the vacuum pickup's nozzle size. Is it large enough? Is it too large? Is it too small?

Switches tend to be larger than many SMT parts and therefore may require a larger nozzle. Also, most typical DIP switches have a polyimide tape seal over the top of the part, which provides enough of a flat surface area for the nozzle to pick it up. Consequently, without the tape seal, or with a too-small part, engineers may find that they have too large a nozzle and run into problems with vacuum pickup. There must be some level of flexibility—the ability to change nozzles sizes, for example.

Also, it's important to consider how the part is oriented in the tape and whether there's enough flat surface area on the switch to allow the part to be taken up cleanly and consistently. The pickup capability for the switch must be compatible with that of other components being placed on the board. It's undesirable to specify a switch that's completely different from the other components in your board, and then find out you lack the proper nozzle with which to pick it up.

It might be thought that such a situation is a "no-brainer," but it occurs quite frequently. A board is primarily populated with resistors, capacitors, and perhaps a few small ICs. Selecting the placement nozzle depends on product size, which may be 1 to 2 mm. Most switches are relatively light, but compared to a chip capacitor or a small integrated circuit, they're massive. Many designers have been frustrated by trying to pick up an electromechanical component with the same nozzle used for capacitors and other smaller, lighter parts.

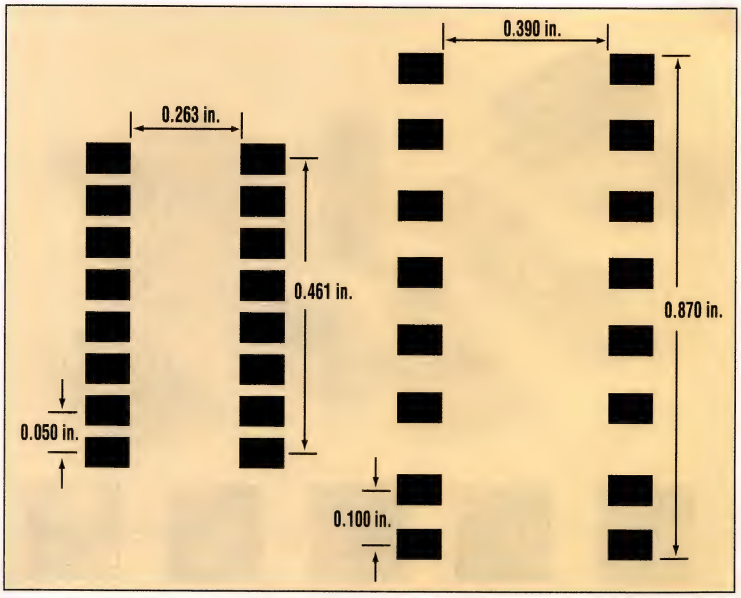
When it comes to many electromechanical components and switches, the engineer can choose a completely sealed product or what's referred to as an open-frame or open-contact device. A sealed product is generally much more compatible with SMT processes. Currently, the sealed product is used more than the open, or non-sealed, product.

Non-sealed products are more vulnerable to production problems than sealed ones. If an SMT process isn't completely under control, flux contamination could be a problem. Or, if the solution used for board cleaning is unfiltered, this may get into the switch or the electromechanical product. In the case of a switch, when that dirty water dries, the potential exists for contamination of the switch contacts, leading to a temporary intermittent switch. If the switch is the type that cleans itself by means of rotation, the contamination may pop up again when it sits for a while. Users may experience this "ghost intermittency" throughout that product's life.

Be it an SMT or leaded device, it's possible to get flux inside of the switch if it isn't sealed. Depending on the type of flux, it can solidify inside the switch and become the major contributor to erratic intermittent switching problems. The other contributor is contaminated washing solution. Either way, the end result is the same. If those contaminants happen to dry on the switch contact surface, the contacts' inherent wiping action may not be enough to get rid of it.

With sealed components, the potential for contamination is practically eliminated. In the case of switches, whether they be toggles or rotaries, they're typically sealed with O rings. DIP switches often have temporary tape seals that will get the device through the processing cycle. With most DIP switches, the tape is placed over the actuators to prevent any contamination or flux intrusion. When the switch has to be set, the tape is broken to set the actuators, making the seal no longer intact.

This doesn't occur with a rotary or toggle switch equipped with an O-ring seal as part of the



3. While many SMT switches are still on a 0.100-in. terminal lead spacing, newer products typically have 0.050-in. lead spacing. This is to save space as well as for processing convenience. The narrower spacing makes the switches compatible with typical board layouts made necessary by most other SMT devices.

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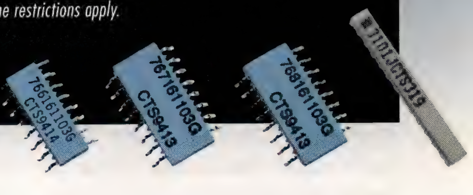

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switch housing. In this case, no matter how many times the rotary or toggle switch is set, the seal remains intact.

This should not be misconstrued to mean that tape seals are inefficient. In fact, they're so effective that sometimes they can't be easily removed. Where the tape seal over the actuators is flush with each end of the DIP switch, the user sometimes is unable to get the tape off the switch unless it goes through processing. It may become necessary to take a small blade and attempt to pry off the tape without harming the part. This situation is rectified by using tape with a small tab that overhangs over an end of the part. From a production viewpoint, a product that has the tab at the end of the tape saves time and averts a certain amount of accidental damage caused by the attempt to remove stubborn tape seals.

Cleaning systems are using higher washing pressures than ever before. Historically, the normal pressure for a cleaning system was between 40 and 50 psi. Now, more systems are using 70 to 80 psi. This is so for a couple of reasons. With high-population boards that use very fine line pitches in their layout, it's critical that everything be thoroughly cleaned. The preferred way to do this is to increase the spray pressure of the cleansing agent.

The engineer must be sure that the devices on the board can withstand the abuse of high-pressure washing from the standpoints of sealing and physical integrity. For example, if high-pressure washing is directly applied to an open switch, it could damage the contacts.

Engineers at Mepcopal have tested a number of switches to determine whether their tape seals could handle the strain of repeated exposure to processing. Depending on the configuration, the component might be able to handle it once or twice, but not a third time. There also can be problems with the seal.

The key is to ensure that the selected switch's seal is robust enough to withstand a high-pressure spray system without degrading and lifting off. Another point to keep in mind is that as the part gets smaller, a tape seal has less surface area to adhere to the part, increasing the chance that it may be worked loose.

Another selection criteria is whether to use gold or solder for terminal plating. Although more expensive, gold has historically been the material of preference due to the low contact-resistance requirements of most low-level circuits. Cost is no longer a major consideration with today's switches because very little gold is needed for the very small contact areas or for selective plating.

From Mepcopal's customer experience, as well as some preliminary documentation, it appears that gold-plating leads may not be the best choice for the SMT environment, because it may lead to brittle solder-joint formation. Evaluation of semiconductor devices has resulted in a move away from gold-plated leads if they're to be soldered to the board. A major user of SMT components will no longer specify devices with gold-plated leads because of the potential for soldering difficulties. Users instead are turning toward components with solder-plated leads, tin-dipped leads, or anything else that's compatible with the solder pads.

Designers should be aware that manufacturers in the U.S., Europe, and the Far East tend to process their boards differently. In the European community, for example, boards are rarely washed after the soldering process. In the U.S., about 90% of OEMs wash the boards after soldering. In particular, designers should be cognizant of this when they select components, especially if that component may end up in a board processed in another country.

Thankfully, materials aren't a concern for users of SMT switches. In the early days of SMT switches, some of the devices that were called "surface-mount" were basically modified leaded products. Many of those consisted of low-temperature materials and were damaged by the higher temperatures required in SMT manufacturing processes. The industry has evolved beyond that today, and materials considerations are no longer a factor.

Materials aren't a concern for users of SMT switches . . . the industry has evolved.

It should be noted, however, that some customers—particularly very large companies—are concerned about flammability. That is, they want UL ratings on the different materials used in the switches. Then they can meet environmental and safety requirements for the end equipment that the switches are built into.

To conclude, the new generation of miniature SMT switches offers the designer the advantage of miniaturization without the sacrifice of process compatibility. Today's tape-seal designs have proven their capabilities for high integrity through testing by various manufacturers. As a result, designers can develop more compact circuitry with components designed for automated SMT assembly that support end-product miniaturization design objectives and board real-estate savings, while providing a high board-manufacturing yield.

Lyle Fette, Mepcopal's director of marketing and sales, holds a BA in economics and an MBA in marketing from the University of Northern Iowa, Cedar Falls.

Tom Gehrman, an applications engineer at Mepcopal, holds a BS in business marketing from San Diego State University and an AA in electronics from Pacific Coast College, San Diego, Calif.

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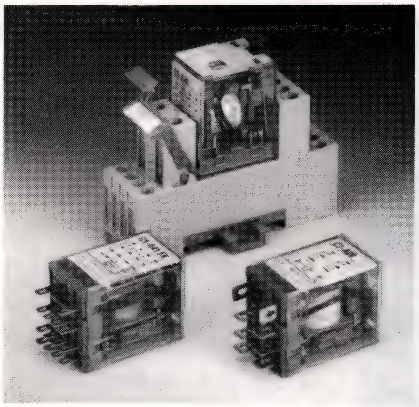

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(continued on p. 113)

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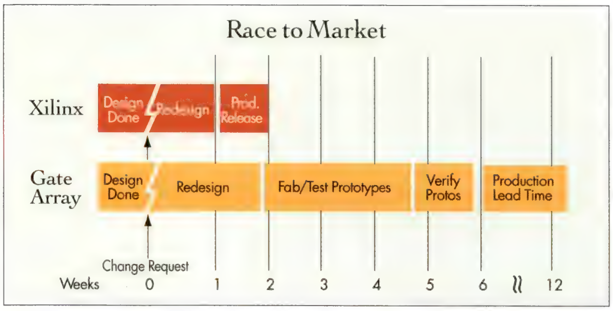

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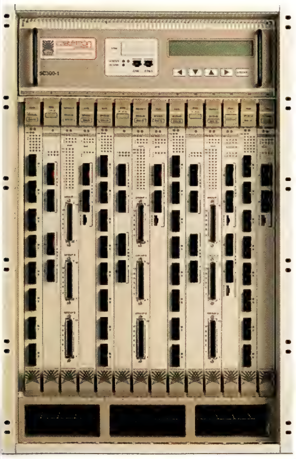

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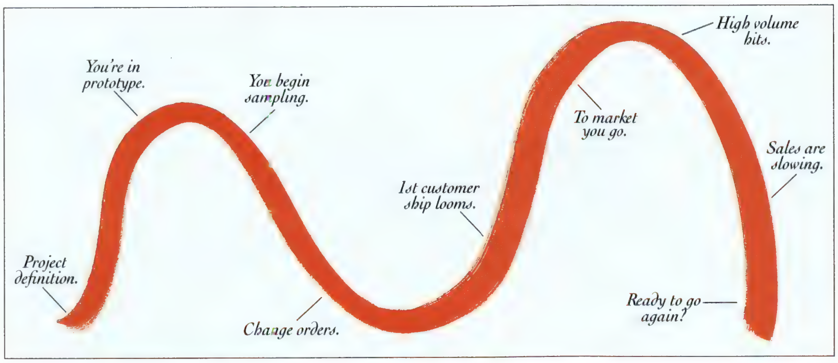

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(AS) (CS) (DS) (HS) (MI) (PW)
CIRCLE 837

GlobTek Inc.
186 Veteran's Dr.
Northvale, NJ 07647
(201) 784-1000
(IL) (PC) (PU) (RK) (RO) (SL)
(SA) (TH) (TG) (AS) (DS)
CIRCLE 838

Gordon Engineering
67 Del Mar Dr.
Brookfield, CT 06804
(203) 775-4501
(PX)
CIRCLE 839

Grayhill Inc.
561 Hillgrove Ave.
P.O. Box 10373
La Grange, IL 60525
(708) 482-2132
(DP) (KB) (KL) (PC)
(PU) (RO) (SM) (AS) (DS)
(IO) (OI) (PB) (PW)
CIRCLE 840

Hallmark Technologies Inc.
1717 E. Lincoln Ave.
Mt. Dora, FL 32757
(904) 383-8142
(KB) (MB) (SA)
CIRCLE 841

Hasco Components Int'l. Corp.
247-40 Jericho Tpke.
Floral Park, NY 11001
(516) 328-9292
(MR) (AU) (DR) (FP) (HD)
(HS) (PB) (PW) (TE)
CIRCLE 842

Haydon Switch & Instrument Inc.
1500 Meriden Rd.
Waterbury, CT 06705
(203) 756-7441
(LI) (PU) (RK) (SA) (TG)
CIRCLE 843

Hermetic Switch Inc.
P.O. Box 1325
3100 Hwy. 92 S.
Chickasha, OK 73023
(405) 224-4046
(LI) (PX) (DR)
CIRCLE 844

Honeywell
Micro Switch
11 W. Spring St.
Freeport, IL 61032
(800) 537-6945
(AP) (IL) (KB) (KL) (LI) (MR)
(PC) (PH) (PS) (PX) (PU) (RK)
(RO) (SA) (SM) (TG)
CIRCLE 845

ITW Switches
6615 W. Irving Park Rd.
Chicago, IL 60634
(312) 282-4040
(IL) (LI) (PC) (PU) (RK)
(RO) (SL) (SA) (SM)
CIRCLE 846

IVO Industries Inc.
34 Industial Way East
Eatontown, NJ 07724
(908) 542-5151
(PH) (PX)
CIRCLE 847

Inresco Inc.
2411 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-6330
(MB) (PX) (DR) (MW)
CIRCLE 848

International Rectifier
Advanced Products Dept.
233 Kansas St.
El Segundo, CA 90245
(310) 607-8862
(AS) (DS) (OI) (PB) (TE)
CIRCLE 849

Janco Corp.
3111 Winona Ave.
Burbank, CA 91504-0038
(818) 846-1800
(IL) (KL) (PC) (PG) (PU) (RO)
CIRCLE 850

Joslyn Jennings Corp.
Jennings Div.
970 McLaughlin Ave.
San Jose, CA 95122
(408) 292-0358
(CO) (CX) (CT) (CS)
(HF) (MI) (PW)
CIRCLE 851

Kilovac Corp.
P.O. Box 4422
Santa Barbara, CA 93140
(805) 684-4560
(AU) (CT) (HD) (HS) (HF) (IO)
(ML) (MI) (PB) (PW)
CIRCLE 852

Lamb Industries Inc.
4826 S.W. Scholls Ferry Rd.
Portland, OR 97225
(503) 297-8878
(AP) (DP) (IL) (KB)
(PC) (PU) (RK) (RO)
(SL) (SA) (SM) (TG)
CIRCLE 853

Littelfuse Inc.
800 E. Northwest Hwy.
Des Plaines, IL 60016
(708) 824-1188
(PU) (AU)
CIRCLE 854

MGR Industries Inc.
450 B Industrial Dr.
Fort Collins, CO 80524
(303) 221-2201
(IL) (KB) (MB) (PU)
CIRCLE 855

MORS/ASC
P.O. Box 544
Wakefield, MA 01880
(617) 246-1007
(DP) (IL) (KL) (PC) (PG) (PU)
(RK) (RO) (SL) (SA) (SM)
(TH) (TG) (TS) (PB)
CIRCLE 856

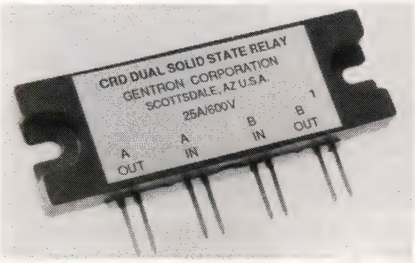
Mantex Corp.
Electronics Div.
P.O. Box 15
Oxford, MI 48371
(810) 628-8210
(MB) (PC)
CIRCLE 857

(see p. 116 for key)

(continued on p. 114)

▼ SOLID-STATE RELAYS ARE SURFACE-MOUNTABLE

Large amounts of power can be controlled with a low-level, dc logic-input signal by the CRD Series of ac solid-state relays. The dual relays are pc-board- or surface-mountable. They incorporate a dual-SCR design to provide full-wave control and high-current capability with high dV/dt capability. Their zero-crossing circuitry switches on at zero voltage and off at zero current for superior switching of inductive loads. The company's Powertherm process allows for better thermal performance, which translates into cooler-running devices and higher reliability. Call for pricing and delivery information.



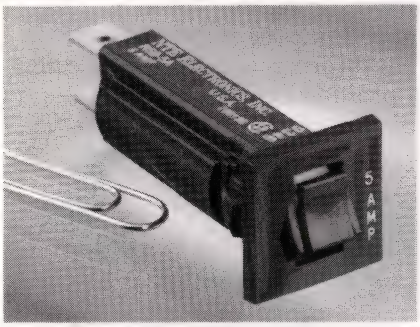
Gentron Corp.
7345 E. Acoma, Suite 101
Scottsdale, AZ 85260
(800) 436-8766
▶CIRCLE 555

▼ SUBMINI PCB RELAY SUITS HIGH-DENSITY USES

Compact size, low heat generation, and good magnetic isolation are features of the V23026 Series of relays. The 1 Form C (SPDT) units are sealed into washable plastic cases measuring 0.51 by 0.30 by 0.27 in. cases. Through-hole and SMT versions of these dc-coil relays are offered. Single- and dual-coil latching models are available, as are non-latching types. Nominal coil power is as low as 30 mW for the 3-V dc single-coil latching models. The devices' bifurcated contacts can switch up to 30 W dc or 60 VA ac. Maximum switched current is 1 A dc or ac, while maximum switched voltage is 150 V dc or 125 V ac. Non-latching, through-hole models cost as little as $1.53 in lots of 10,000. Call for delivery information.

Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671-0001
(812) 386-2257
▶CIRCLE 556

▼ THERMAL BREAKER REPLACES GLASS FUSES



Specially designed to replace slow-blow glass-cartridge fuses, the R59 Series thermal circuit breakers feature 0.250-in. quick-connect terminals, snap-in mounting, visual trip indication, and a reset button. All 14 devices in the series are UL- and CSA-rated. Current ratings range from 0.25 to 20 A. Maximum voltages are 32 V dc and 250 V ac, and dielectric strength is 1500 V ac rms. The units can carry 100% of rated current continuously. Call for pricing and delivery information.

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
▶CIRCLE 557

▼ 1/2-IN. SMT SWITCH WITHSTANDS PROCESSING

Surface-mounted switches are typically sensitive to SMT processing and often require separate handling. The SMS Series switches, however, feature insert-molded, tin-plated terminals that are compatible with processes used to mount other SMT devices. They resist 260°C soldering for 10 seconds. Solderability is 235°C for two seconds. The 1/2-in. size allows for greater heat resistance as well as longer electrical and mechanical life. Rated current and voltage is 50 mA at 30 V ac/42 V dc for switches with silver contacts. Contact travel is 0.35 mm. Switches are offered with J-style, gullwing, or through-hole leads. Prices start at $0.68 in lots of 500. Delivery is from stock to eight weeks.

Schurter Inc.
1016 Clegg Ct.
Petaluma, CA 94954
(707) 778-6311
▶CIRCLE 558

SWITCH AND RELAY MANUFACTURERS

Marquardt Switches Inc.
2711 Route 20E
Cazenovia, NY 13035
(315) 655-8050
(KB) (PU) (RK) (SL)
(SA) (TG)
CIRCLE 858

Matrix Systems Corp.
5177 N. Douglas Fir Rd.
Calabasas, CA 91302
(818) 222-2301
(CX) (DR) (HS) (MW) (TE)
CIRCLE 859

McGill Electric Switch Group
1002 N. Campbell St.
Valparaiso, IN 46383
(219) 465-2379
(PU) (RK) (SA) (TG)
CIRCLE 860

Micropac Industries Inc.
Solid State Relays Div.
P.O. Box 469017
Garland, TX 75046
(214) 272-3571
(AS) (DS) (MI) (OI) (PW)
CIRCLE 861

Molex Inc.
Switch Products Div.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
(MB) (PU)
CIRCLE 862

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
(DP) (IL) (KL) (PC) (PU) (RK)
(RO) (SL) (SM) (TG)
CIRCLE 863

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(AS) (AU) (DS) (DR) (FP)
(IO) (PB) (PW) (TD)
CIRCLE 864

Norstat Inc.
300 Roundhill Dr., Unit 4
Rockaway, NJ 07866
(201) 586-2500
(AS) (CS) (IO) (TD) (VS)
CIRCLE 865

OakGrigsby Inc.
88 N. Dugan Rd.
Sugar Grove, IL 60554-0890
(708) 556-4200
(IL) (KL) (PC) (PG) (PU) (RO)
CIRCLE 866

Omega Engineering Inc.
One Omega Dr.
Stamford, CT 06907
(203) 359-1660
(AC) (AP) (LI) (MR) (PC)
(PG) (PX) (RO) (CT) (CŞ)
(DS) (DF) (DR) (IO) (ML)
(MW) (RT) (VS)
CIRCLE 867

Omron Electronics Inc.
One E. Commerce Dr.
Schaumburg, IL 60173
(800) 843-8081
(DP) (IL) (KL) (LI) (PC) (PH)
(PX) (PU) (RK) (RO) (SA)
(SM) (TH) (TS) (AS) (AU)
(CS) (DS) (HD) (IO) (ML) (OI)
(PB) (PW) (TE) (TD) (VS)
CIRCLE 868

Opto 22
43044 Business Park Dr.
Temecula, CA 92557
(909) 695-9299
(AS) (DS) (FP) (HD) (HS) (IO)
(MW) (MI) (OI) (PB) (PW)
CIRCLE 869

Original Electric Mfg. Co. Inc.
600 Lincoln Blvd.
Middlesex, NJ 08846
(908) 271-5770
(AU) (DR) (FP) (PW) (TE)
CIRCLE 870

Oslo Controls Inc.
328 Industrial Ave.
Cheshire, CT 06410
(203) 272-2794
(IL) (KL) (PU) (RK)
CIRCLE 871

Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671-0001
(812) 386-2316
(AS) (AU) (CT) (CS) (DS)
(DR) (FP) (HD) (HS) (IO) (ML)
(MW) (OI) (PB) (PW) (RT)
(TE) (TD) (VS)
CIRCLE 872

Pres:Air:Trol Corp.
1009 W. Boston Post Rd.
Mamaroneck, NY 10543
(914) 698-2026
(AP)
CIRCLE 873

PrimeSource Components
57 Stanley Ave.
Watertown, MA 02172-4802
(617) 926-0011
CIRCLE 874

Raltron Electronics Corp.
2315 N.W. 107th Ave.
Miami, FL 33172
(305) 593-6033
(DP) (PC) (SM)
CIRCLE 875

Robert Bosch Corp.
Automotive Group
P.O. Box 4601
Carol Stream, IL 60197-4601
(708) 865-5301
(AU)
CIRCLE 876

SAGER Electronics
60 Research Rd.
Hingham, MA 02043
(800) 724-3780
(DP) (IL) (KB) (KL) (LI) (MR)
(MB) (PC) (PH) (PS) (PX)
(PU) (RK) (RO) (SL) (SA)
(SM) (TH) (TG) (TS) (AS)
(AU) (CT) (CS) (DS) (DR)
(HD) (HS) (HF) (IO) (ML)
(MW) (MI) (OI) (PB) (PW)
(RT) (TE) (TD) (VS)
CIRCLE 877

SECMA Inc.
17752 Skypark Cir. #200
Irvine, CA 92714
(714) 261-0610
(DP) (IL) (KB) (PC) (PS) (PU)
(RO) (SA) (SM) (TH) (TG)
CIRCLE 878

SSAC Inc.
P.O. Box 1000
Baldwinsville, NY 13027
(315) 638-1300
(PH) (AS) (CS) (OI) (TD) (VS)
CIRCLE 879

Schurter Inc.
1016 Clegg Ct.
Petaluma, CA 94954
(800) 848-2600, ext. 199
(IL) (KB) (MB) (PC) (PU)
(RK) (RO) (SA) (ST) (SM)
CIRCLE 880

Seco-Larm
17811 Skypark Cir.
Suites D & E
Irvine, CA 92714
(714) 261-2999
(KL) (MR) (PU)
CIRCLE 881

Shallco Inc.
308 Components Dr.
Smithfield, NC 27577
(919) 934-3135
(DP) (KL) (RO)
CIRCLE 882

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021-4799
(516) 466-0911
(PC) (PU) (RK) (SL) (TG)
CIRCLE 883

Silver Cloud Mfg.
525 Orange St.
Millville, NJ 08332
(609) 825-8900
(KB) (MB) (PC) (SA)
CIRCLE 884

SoLiCo/MEC
75 Locust St.
Hartford, CT 06114
(203) 527-3092
(PC) (PU) (SM)
CIRCLE 885

Staco Switch Inc.
1139 Baker St.
Costa Mesa, CA 92627
(714) 549-3041
(IL) (KB) (PU)
CIRCLE 886

Switchcraft Inc.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
(IL) (KB) (PC) (PU)
(RK) (SL) (TG)
CIRCLE 887

Tapeswitch Corp.
100 Schmitt Blvd.
Farmingdale, NY 11735
(516) 694-6312
(IL) (LI) (SA)
CIRCLE 888

Teledyne Inc.
Solid State Div.
12525 Daphne Ave.
Hawthorne, CA 90250
(213) 777-0077
(AS) (DS) (HS) (IO) (MI) (OI)
CIRCLE 889

Teledyne Microelectronics
12964 Panama St.
Los Angeles, CA 90066
(213) 822-8229
(DP) (PC) (SM) (HS) (HF)
(ML) (OI) (DS) (TD)
CIRCLE 890

Teledyne Relays
12525 Daphne Ave.
Hawthorne, CA 90250
(213) 777-0077
(HS) (HF) (ML) (MI) (PB)
CIRCLE 891

(see p. 116 for key)

(continued on p. 116)

WHAT'S SO SPECIAL ABOUT

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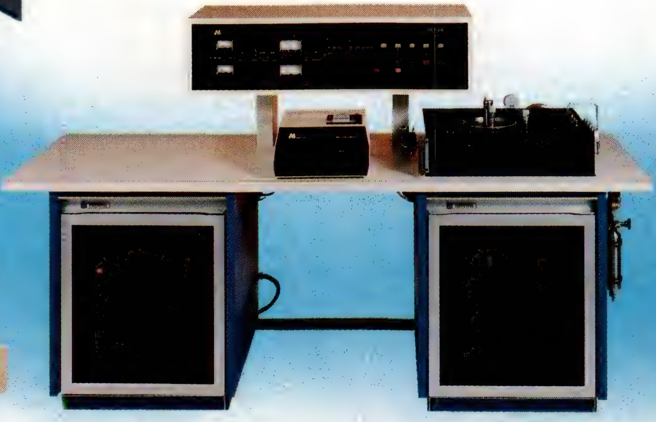
Custom Fabrication is a Standard



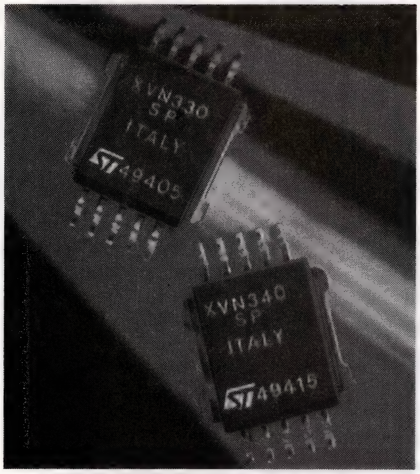
BUD INDUSTRIES, INC.

BUD INDUSTRIES, INC. ▪ 4605 E. 355TH Street ▪ P.O. Box 998
Willoughby, Ohio 44094 ▪ (216) 946-3200 ▪ Fax (216) 951-4015

BUD WEST ▪ P.O. Box 1029 ▪ Peoria, Arizona 85245-0350
(602)979-0300 ▪ Fax (602) 878-5371

READER SERVICE 84

▼ QUAD SS RELAYS ARE SMT-COMPATIBLE



Two solid-state relays feature four independent high-side switches housed in a PowerSO-10 surface-mount package. Built with the company's VIPower technology, the VN330SP amd VN340SP relays contain integrated control and diagnostic circuitry along with four 200-mΩ vertical DMOS power transistors, each of which can drive resistive or inductive loads with one side connected to ground. Features include automatic protection circuitry and a status output that enables an external controller to determine whether a fault has occured. Protection is provided against undervoltage conditions, load short circuits, and excessive temperature. Call for pricing and delivery information.

SGS-THOMSON Microelectronics Inc.
55 Old Bedford Rd.
Lincoln, MA 01773
(617) 259-0300
▶CIRCLE 559

▼ SUBMINI PUSHBUTTONS GIVE TACTILE FEEDBACK

A positive detent is featured in the KC Series subminiature tactile pushbutton switches. The high-reliability devices offer a momentary, normally open, SPST function. Four actuator heights range from 0.028 to 0.232 in. high. Three standard terminal styles include pc-mount, pc-mount with an ESD pin, and a right-angle version. All terminals are insert-molded and silver-plated. Ratings are 0.6 VA maximum at 12 V ac or dc maximum. Electrical life is 100,000 make-and-break cycles minimum at full load. Contact resistance is below 100 mΩ typical, initially, at 2 to 4 V dc, 100 mA. Pricing starts at $0.24 in lots of 1000. Delivery is from stock to six weeks.

C&K Components Inc.
57 Stanley Ave.
Watertown, MA 02172-4802
(617) 926-6400
▶CIRCLE 560

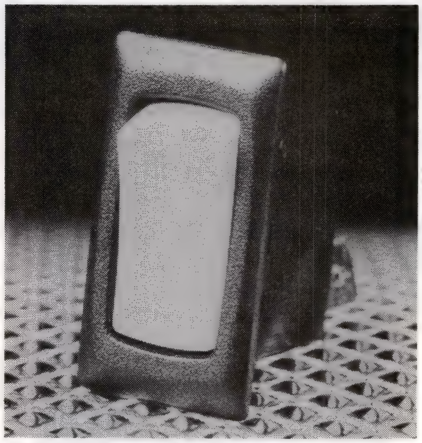
▼ TACTILE SWITCHES COME IN WIDE ARRAY

A full line of mechanical tactile switches offers a vast array of actuators and terminations, giving designers flexibility in applications. The switch function is SPST-NO with a contact rating of 50 mA at 12 V dc. There are four basic styles: the PTS635 (6 by 3.5 mm), the PTS435 (4.5 mm^2), the PTS645 (6 mm^2), and the PTS125 (12 mm^2). The PTS635 and PTS435 are rated for 50,000 cycles. The PTS645 is rated for 100,000 cycles, and the PTS125 is rated for 500,000 cycles. Prices start at $0.15 in lots of 10,000. Delivery is from stock to six weeks. Call for samples and literature.

PrimeSource Components
57 Stanley Ave.
Watertown, MA 02172
(617) 926-0011
▶CIRCLE 561

▼ CIRCUIT BREAKER LIGHTS ON OVERLOAD

A small, fast-tripping circuit breaker illuminates under tripped conditions. The Series 1410-F breaker is now available as a combined rocker switch/circuit breaker for snap-in panel mounting. Its rocker switch carries an internal red indicator light that immediately lets the user know that power has been lost due to a tripped breaker. The unit's fast trip characteristics make it suitable for a wide range of applications. Current ratings range from 0.63 to 8 A. Call for pricing and delivery information.



E-T-A Circuit Breakers
7400 N. Croname Rd.
Niles, IL 60714-3982
(708) 647-8303
▶CIRCLE 562

SWITCH AND RELAY MANUFACTURERS

Topflight Corp.
Membrane Switch Div.
935 Borom Rd.
York, PA 17404
(717) 764-8237
(IL) (KB) (MB) (SA)
CIRCLE 892

Tricon Industries Inc.
Electromechanical Div.
1600 Eisenhower Ln.
Suite 200
Lisle, IL 60532-2167
(708) 964-2330
(PU) (SA)
CIRCLE 893

Veetronix Inc.
Reach Electronic Inc.
1000 Washington St.
Lexington, NE 68850
(308) 324-4600
(IL) (KB) (MR) (PC) (PU) (SM)
CIRCLE 894

Wilbrecht Electronics Inc.
1400 Energy Park Dr.
St. Paul, MN 55108
(612) 659-0919
(PC) (PU) (SL)
CIRCLE 895

Xymos Technologies Inc.
8225 W. Parkland Ct.
Milwaukee, WI 53202
(800) 869-9669
(KB) (MB)
CIRCLE 896

KEY

Switches

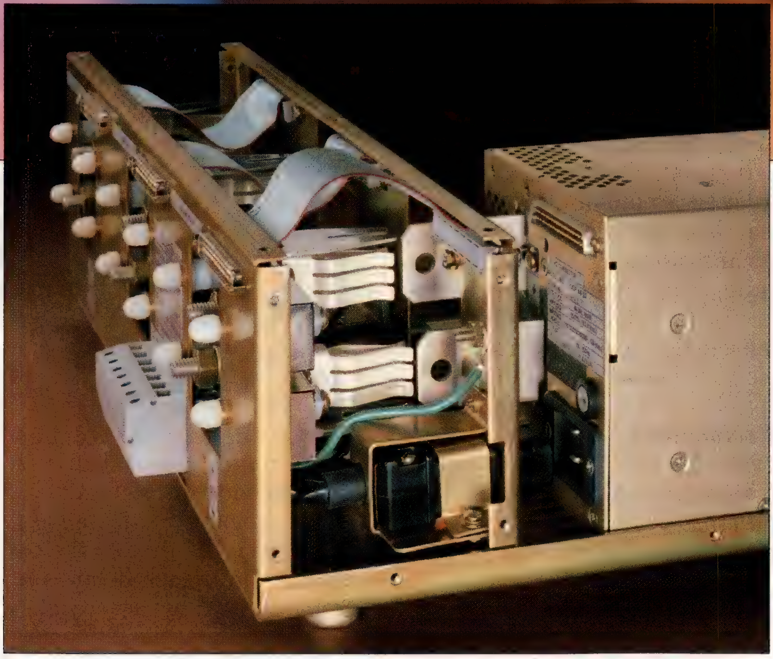
(AC)	Acceleration
(AP)	Air-pressure
(CO)	Coaxial
(DP)	DIP
(IL)	Illuminated
(KB)	Keyboard
(KL)	Keylock
(LI)	Limit
(MR)	Magnetic reed
(MB)	Membrane
(PC)	Pc-mounted
(PH)	Photoelectric
(PS)	Piezoelectric
(PG)	Programmable
(PX)	Proximity
(PU)	Pushbutton
(RK)	Rocker
(RO)	Rotary
(SL)	Slide
(SA)	Snap-action
(ST)	Stepping
(SM)	Surface-mounted
(TH)	Thumbwheel
(TG)	Toggle
(TS)	Touch screens

Relays

(AS)	Ac solid-state
(AU)	Automotive
(CX)	Coaxial
(CT)	Contactors
(CC)	Crystal-case
(CS)	Current-sensing
(DS)	Dc solid-state
(DF)	Differential
(DR)	Dry reed
(FP)	Flat-pack
(HD)	Heavy-duty
(HS)	Hermetically sealed
(HF)	High-frequency
(IO)	Input/output
(ML)	Magnetic latching
(MW)	Mercury-wetted reed
(MI)	Military/aerospace
(OI)	Optical isolation
(PB)	Pc-board
(PW)	Power
(RT)	Rotary
(TE)	Telephone
(TD)	Time-delay
(VS)	Voltage-sensing

PSSSST!
WANNA BUY A HOT SWAP?

Sure you do, if your job needs the reliability of a redundant power supply. Kepco's 1000W HSP high-frequency switchers have all the goodies you need:



Rear view, cover removed, of the rack housing showing the heavy-duty bus-bar connections that make HSP's "Hot Swap" practical. Note: The a-c input connector has a mating connector, too.

- Forced Current Sharing
- Wide Range a-c Input, 90-264V a-c
- Power Factor Correction, 0.98
- Plug-in Rack Housings, 3-4 units
- Preset output for seamless substitution while your bus is HOT
- Built-in EMI filtering (FCC Class A)
- Meet ANSI C62.41 (near lightning strikes).

Other Models Available for N+1 Redundancy, from 50 Watts.

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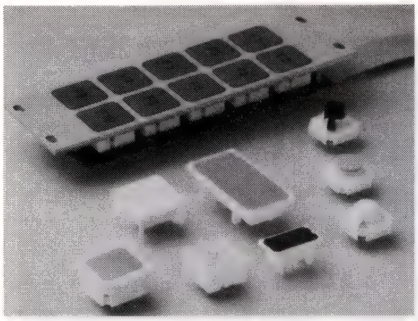
Western Region, 800 West Airport Freeway, Suite 320, LB 6018, Irving, TX 75062 USA • Tel: (214) 579-7746 • Fax: 579-4608

See us at Electronica,Kepco Booth 24B29

READER SERVICE 166

▼ KEYSWITCH MODULES FEATURE SNAP ACTION

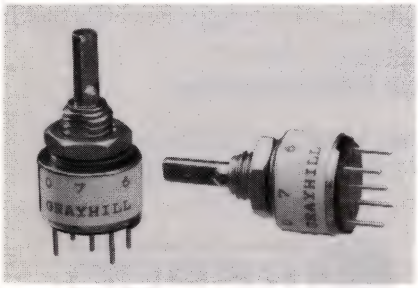
The distinctive tactile feel and audible click of a short-travel switch is embodied in the RF 15/19 switch modules. The modules solder-mount to a circuit-card assembly and are used with a tough polyester membrane overlay. Modular in nature, the low-profile RF 15 (15 mm^2) and RF 19 (19 mm^2) keyswitches allow for easy custom layouts. The overlay legend is screened on the rear surface to ensure resistance to wear and chemicals. When properly gasket-mounted, the flat membrane permits full environmental sealing to NEMA 13. Various actuator heights are available, as is spot and full integral illumination with red, green, and yellow LEDs. Call for pricing and delivery information.



Industrial Electronic Engineers Inc.
7740 Lemona Ave.
Van Nuys, CA 91409
(818) 787-0311, ext. 418
▶CIRCLE 730

▼ CODED ROTARY SWITCHES TAKE LITTLE SPACE

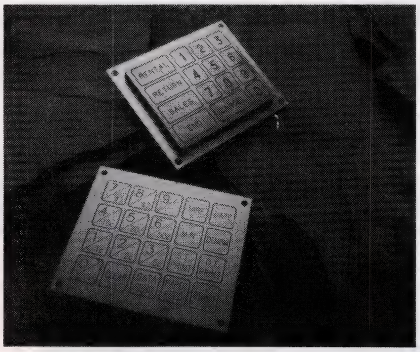
A line of coded-output rotary switches measure just 1/2 in. in diameter and require less than 3/8 in. of depth behind the panel. The Series 26 switches are a low-cost alternative to electronic encoders and thumbwheel switches. Switches are available in BCD-code output in eight and 16 positions and in Gray code with 16 positions. Features include an adjustable stop mechanism. The user can set pins at the front of the switch to select the amount of rotation and the code output. For example, a 16-position BCD-coded switch can be set to rotate between positions 0 and 9 to create a BCD decimal output. Pricing is about $7 in lots of 100.



Grayhill Inc.
561 Hillgrove Ave.
La Grange, IL 60525
(708) 482-2132
▶CIRCLE 731

▼ SEALED SWITCHES CAN TAKE ABUSE

The Indestructible line of electronics switches, keypads, keyboards, and control panels is designed to endure the harshest environmental abuse, thanks to a solid metal construction with no moving parts and complete sealing. Extreme temperatures, moisture, oil, chemicals, vandalism, and even explosions pose little threat, it is claimed. With no moving parts and no material or mechanical fatigue, the switches' life expectancy is virtually eliminated. Tests have taken the devices to in excess of 50 million cycles without failure. Call for pricing and delivery information.



Everswitch USA
12079 Tech Rd.
Silver Spring, MD 20904
(301) 680-3100
▶CIRCLE 732

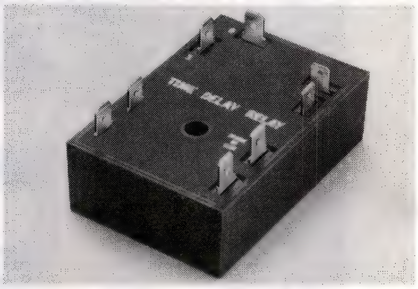
▼ SMT SWITCH LINES COME IN REELS, TUBES

Tape-and-reel and stick-tube packaging is now offered for NKK's microsubminiature G3T toggle and G3B pushbutton switches. The packaging reduces assembly costs by allowing rapid, automatic placement of the switches on pc boards by SMT equipment. Both switch types can be specified in upright, bracketed-upright, and right-angle mounting configurations. Upright-mounting devices come 50 to a stick-tube. Right-angle devices come on a 24-mm-wide tape with 500 pieces to a reel. The devices are totally sealed to prevent contact contamination during board processing. Ratings are 0.4 VA maximum and 28 V ac/dc maximum. SPDT and DPDT configurations are available. Call for pricing and delivery information.

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
▶CIRCLE 733

▼ RECYCLING RELAY CONTROLS UP TO 30 A

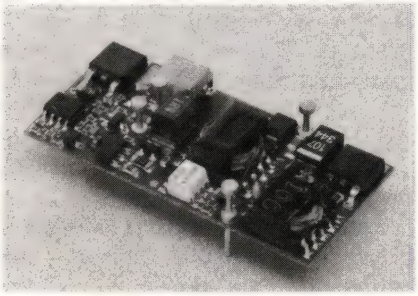
A combination of a power relay and a digital, solid-state timing circuit comprises the HRDR Series recycling time-delay relays. Output contacts are rated at 30 A resistive, 1 hp, 125 V ac, making the devices suitable for direct control of pumps, compressors, fans, heaters, and lamps. Five time ranges are available from 200 milliseconds to 100 minutes. Delays can be remotely adjusted or factory-fixed. The ON time or the OFF time can be first; each delay is adjusted separately. A bypass/reset switch is pushed (at any time) to energize the output and reset the time delays. Opening the switch restarts the recycling operation with the first delay. Call for pricing and delivery information.



SSAC Inc.
P.O. Box 1000
Baldwinsville, NY 13027
(315) 638-1300
▶CIRCLE 734

▼ WIDE-INPUT CONVERTERS TARGET TELECOM USES

The BX10 Series of dc-dc converters targets telecommunication applications with 10 W of output in a 1-by-2-by-0.375-in. package, yielding a power density of more than 13 W/in.^{3}. The converters accept inputs of either 18 to 75 V dc or 9 to 36 V dc and provide regulated, single- and dual-output voltages of 2.1, 3.3, 5, 12, 15, ±5, ±12, and ±15 V. Efficiencies are as high as 88% on 12-V output units and 79% on 3.3 V. The transient response for a 25% load step is ±2% maximum deviation with a 250-µs recovery to within 1% of the final output voltage. Maximum output ripple and noise are 75 mV p-p and 20 mV rms, respectively. Single-piece pricing starts at less than $50. Call for delivery information.



Computer Products Inc.
7 Elkins St.
South Boston, MA 02127
(617) 464-6656
▶ CIRCLE 735

▼ NiMH BATTERY PACKS BOAST HIGH CAPACITY

Compared to nickel cadmium cells, Varta's line of nickel metal hydride battery packs offer significantly higher capacity, it's claimed. The packs, which are 100% free of cadmium, lead, and mercury, have a high charge density for powering portable applications. The company's NiMH button cells also offer an environmentally compatible solution for bridging and RTC/MBU applications. Nickel cadmium button cells can be directly replaced with no modification to existing charging circuits or pc-board layouts. In lots of 100,000, prices start at $0.57 for single-cell V11H NiMH batteries.

VARTA Batteries Inc.
300 Executive Blvd.
Elmsford, NY 10523
(914) 592-2500
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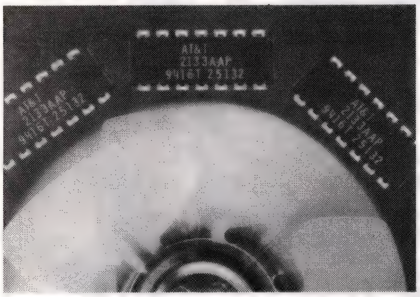
▼ MOTOR-DRIVER IC USES AC-LINE POWER

A low-voltage, single-phase brushless dc motor can be run directly off the ac line when using the ATT2133AAP motor-driver IC. The chip lets designers replace inefficient ac motors with more efficient dc motors without resorting to bulky transformers or a separate dc power supply. It provides complete control and drive to run a brushless dc motor with only an ac-power source. In addition to the direct ac-to-dc conversion, the IC integrates all the necessary commutation logic and drive circuitry. The dc voltage supplied by the IC is user-programmable for maximum flexibility. In addition, the part provides a regulated 8-V output to power a discrete commutating Hall-cell IC. In a 14-pin plastic DIP, the IC goes for less than $2.50 in OEM quantities. Samples and data sheets are available now.



AT&T Microelectronics
Room 21Q-133BA
555 Union Blvd.
Allentown, PA 18103
(800) 372-2447, Dept. P16
▶ CIRCLE 737

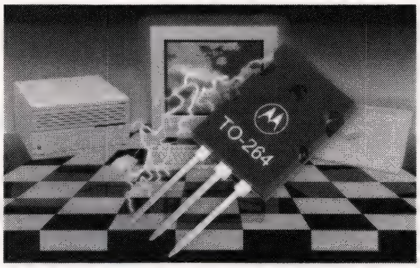
▼ RUGGED 1600-V IGBTs OFFER DURABILITY

With current ratings based on an 80°C baseplate-junction temperature instead of the typical 25°C, the BSM Series of IGBT modules is extremely durable in high-voltage motor-drive and ac-power-system applications. The 1600-V modules are based on non-punch-through technology, making them less vulnerable to failure modes, such as latchups, that can destroy conventional IGBTs at high temperatures. The units owe their ruggedness to Siemens' free-wheeling diode technology, which provides soft-recovery characteristics in the course of operation. Competitive devices may feature an abrupt recovery that can create self-damaging overvoltage spikes. Additional system benefits include lower turn-on power losses and decreased switching noise and EMI. All six devices in the series are designed for different current requirements, from 50 A (BSM 50) to 300 A (BSM 300). Pricing ranges from $78 for the 50-A model to $172 for 150- and 300-A models. Samples are available now.

Siemens Components Inc.
10950 N. Tantau Ave.
Cupertino, CA 95014
(800) 777-4363, ext. 663.
▶ CIRCLE 738

▼ TO-264 POWER MOSFETs MANAGE LOADS TO 5 kW

With a high-voltage, TO-264 family of n-channel TMOS power MOSFETs, designers can safely dissipate 300 W within the devices and control loads of up to 5 kW. The TO-264 package uses a large 315-by-470-mil die and, although it's about 50% larger than a TO-247 package, the pin spacing for the packages is identical. This means that MOSFETs in the TO-264 package can fit in the same mounting holes as a TO-247, making retrofits relatively easy. The current offering includes 500-, 600-, and 1000-V devices. A major advantage is the fact that a single TO-264 part can eliminate the need to parallel multiple TO-247 power MOSFETs to handle higher currents and achieve lower on-resistance values. On-resistance for the 500-V/15-A device is only 140 mΩ compared with 240 mΩ for a 500-V TO-247 MOSFET. Typical applications are found in dc-dc converters, power-factor correction, inverters, uninterruptible power supplies, battery chargers, high-voltage motor drives, and welders. Pricing starts at $5.45 for the 500-V model in lots of 25,000.



Motorola Inc.
5005 E. McDowell Rd.
Phoenix, AZ 85018
(602) 244-3071
▶ CIRCLE 739

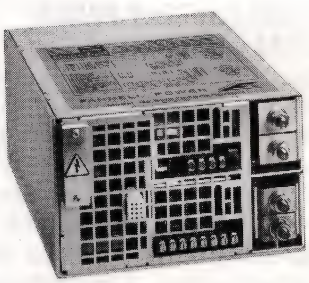
▼ BATTERY-CHARGER IC INCLUDES SELF-TEST

A microprocessor-based, fast battery-charger IC incorporates all the latest charging techniques for NiCd batteries along with extra features for NiMH cells. The ATC106 charger IC includes a self-test feature that tests the critical functions of the charger to confirm that it works properly. Tested features include maximum timer, full-charge indication, ΔT/Δt sensitivity, –ΔV sensitivity, fast-charge mode, discharge mode, buzzer, and LED test. The IC permits easy selection of ΔT/Δt slope rate and automatic or manual discharge. Available packages include a 24-pin shrink DIP and a 24-pin plastic SO. Pricing in lots of 1000 is $3.50. Delivery is from stock.

Shoreline Electronics Inc.
2098B Walsh Ave.
Santa Clara, CA 95050
(408) 987-7733
▶ CIRCLE 740

▼ MULTI-OUTPUT SUPPLIES BOAST CUSTOM OPTIONS

A variety of optional custom features can be appended to the BW Series of multi-output power supplies. The series includes the BWF 2000, a 2000-W, multi-output unit with input of 176 to 240 V ac; and the BWN 1200, a 1200-V single-output type with inputs from 98 to 264 V. Both are power-factor corrected and fan-cooled. The complete series spans single-, dual-, and triple-output units in 3.3-, 5-, 12-, 24-, and 48-V configurations. Options include a ±5% "marginating" output, latching and non-latching inhibit, and logic invert. Call for pricing and delivery.



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Solon, OH 44139
(216) 349-0755
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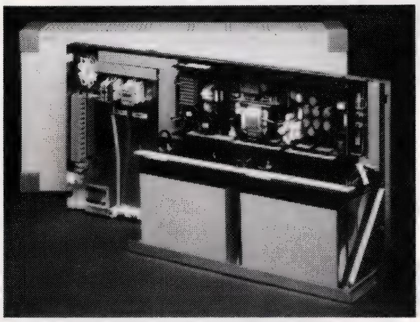
▼ WALL-MOUNTED SYSTEM ENSURES POWER FLOW

A flexible, uninterruptible power system for small PABX applications ensures that systems will receive a continuous power flow. The system comprises a PE 5271 dc UPS installed, along with a battery, in a small wall-mounted box. This design's flexibility is in the fact that customers can specify the required battery size for their application. Up to eight hours of battery power can be accommodated. Unlike standard ac backup systems, this configuration has no inverter. Rather, a rectifier converts the mains voltage to a 300-V dc bus. This cost-effective solution is also more reliable. Call or write for information.



Philips Power Systems
Bd. de l'Europe 131
B 1301 Wavre, Belgium
(32) 10 438502
▶ **CIRCLE 742**

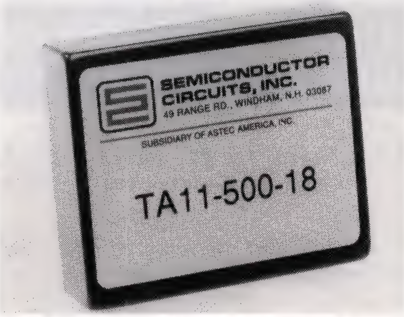
▼ DENSE CONVERTERS OFFER DUAL OUTPUTS

A dual-output, 200-W dc-dc converter with power density approaching 40 W/in.^{3} is being claimed as an industry first. The SM200D converter offers military-system designers access to very-high-density, dual-output building blocks for VME systems or other distributed-power applications without compromising MIL-spec reliability or ruggedness. The unit accepts a nominal 28-V dc input with a range from 18 to 36 V dc. Output voltages are ±5, ±12, and ±15 V dc with maximum current of 15, 8, and 7 A on each output, respectively. Features include current-mode design, fixed-frequency topology, standard components, and surface-mount packaging. Units also offer full component derating to NAVMAT and hermetic/ceramic military-grade ICs. TTL on-off logic is standard and a sync pin is provided for frequency synchronization to other modules or to a system clock. Pricing is from $750.

Abbott Electronics Inc.
2727 S. La Cienega Blvd.
Los Angeles, CA 90034
(310) 202-8820
▶ **CIRCLE 743**

▼ DC-DC CONVERTERS NOW BUILT WITH SMT

The updated TA Series of dc-dc converters now features surface-mount internal construction. The units offer a 25-W output in a 2.5-by-3.0-by-0.83-in. package. Applications include telecommunication equipment as well as others having a widely varying input voltage, such as automotive test equipment, process controls, minicomputers, and geosurvey equipment. Single-, dual-, and triple-output models are available. A 4:1 input range (9 to 36 or 20 to 72 V) is featured as is remote shutdown and a 100-kHz switching frequency. Pricing in OEM lots ranges from $65 to $75 depending on wattage.


SEMICONDUCTOR CIRCUITS, INC.
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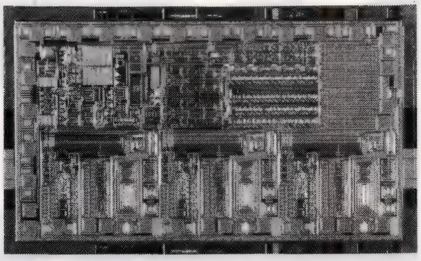
TA11-500-18

Semiconductor Circuits Inc.
49 Range Rd.
Windham, NH 03087
(603) 893-2330
▶ **CIRCLE 744**

▼ SURFACE-MOUNT IC CONTROLS DC MOTORS

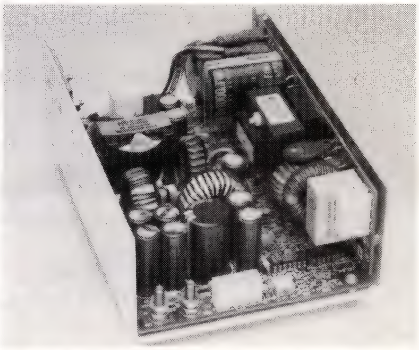
A surface-mount controller IC for three-phase brushless dc motors integrates both the high-side drive and low-voltage-regulator functions. When used as a chip set with the company's Little Foot power MOSFETs, the Si9979CS controller forms a complete, compact, and efficient solution that can be mounted directly on the 20-to-40-V motors used in office equipment and industrial systems. Designed to handle motor currents from 1 to 5 A, the Si9979CS IC integrates more than a dozen control and protection functions. Providing commutation from Hall-effect sensors, the IC is configured to allow either 60° or 120° spacing. Samples and large lots are available now. Pricing in lots of 1000 is $7.09.



Siliconix
2201 Laurelwood Rd
P.O. Box 54951
Santa Clara, CA 95056-0951
(800) 554-5565, ext. 26
▶ **CIRCLE 745**

▼ HIGHLY COMPACT SUPPLIES OFFER OUTPUTS TO 375 W

Power densities up to 4.3 W/in.^{3} are available in the 124 Series of compact, low-density power supplies. Any number of configurations are available depending on requirements. The ac-input range is from 90 to 264 V ac single phase (autoranging). Model 124-01, the first to be configured, operates at a fixed frequency of 85 kHz and offers outputs of 5 V at 35 A, +12 V at 10 A (15 A pk), –12 V at 0.5 A, and –5 V at 0.5 A. There's overvoltage protection on the +5- and +12-V outputs. Pricing is from $225 in lots of 1000.



Conversion Equipment Corp.
330 W. Taft Ave.
Orange, CA 92665
(714) 637-8654
▶ **CIRCLE 746**

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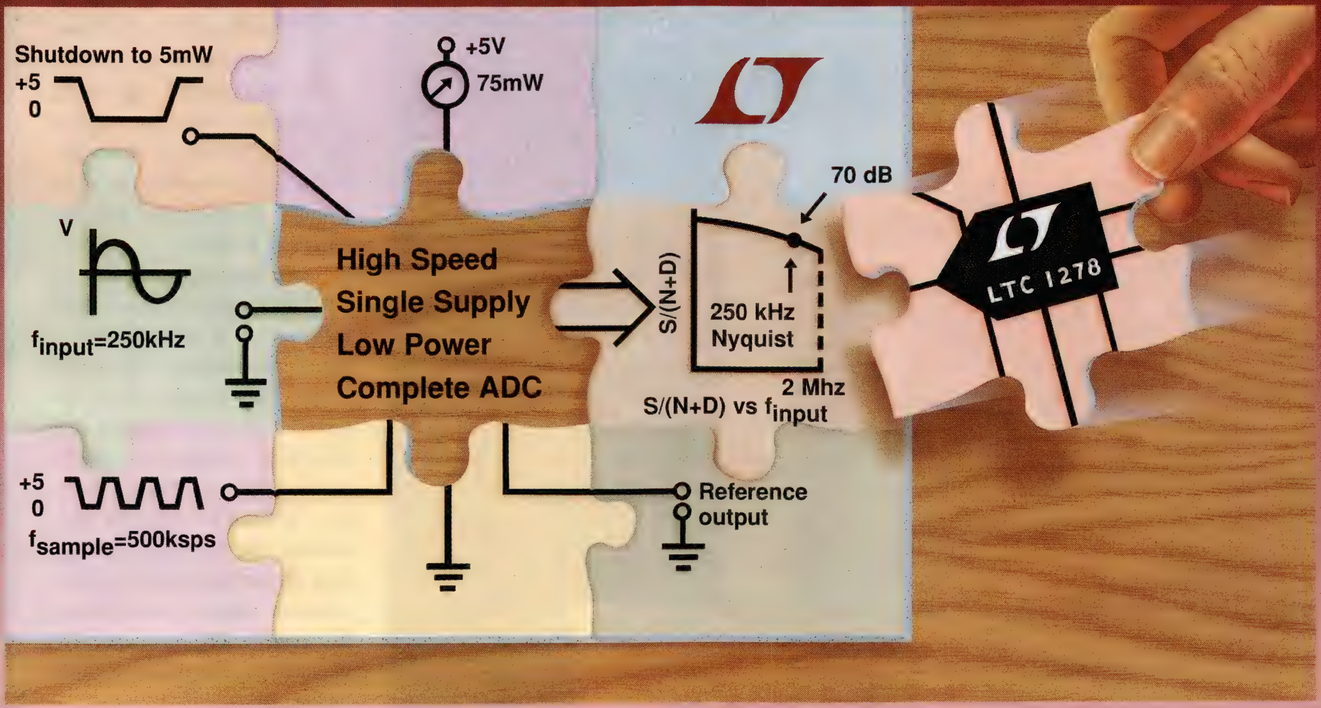

The LTC1278: 12-Bits, 500ksps, single supply and shutdown. The perfect fit.

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LTC1273	300ksps	70dB	5V	75mW	11.75
LTC1275/76	300ksps	70dB	±5V	75mW	11.00
LTC1278	**500ksps**	**70dB**	**5V or ±5V**	**75mW 5mW***	12.85
LTC1282	140ksps	68dB	3V or ±3V	12mW	13.47

*power down mode

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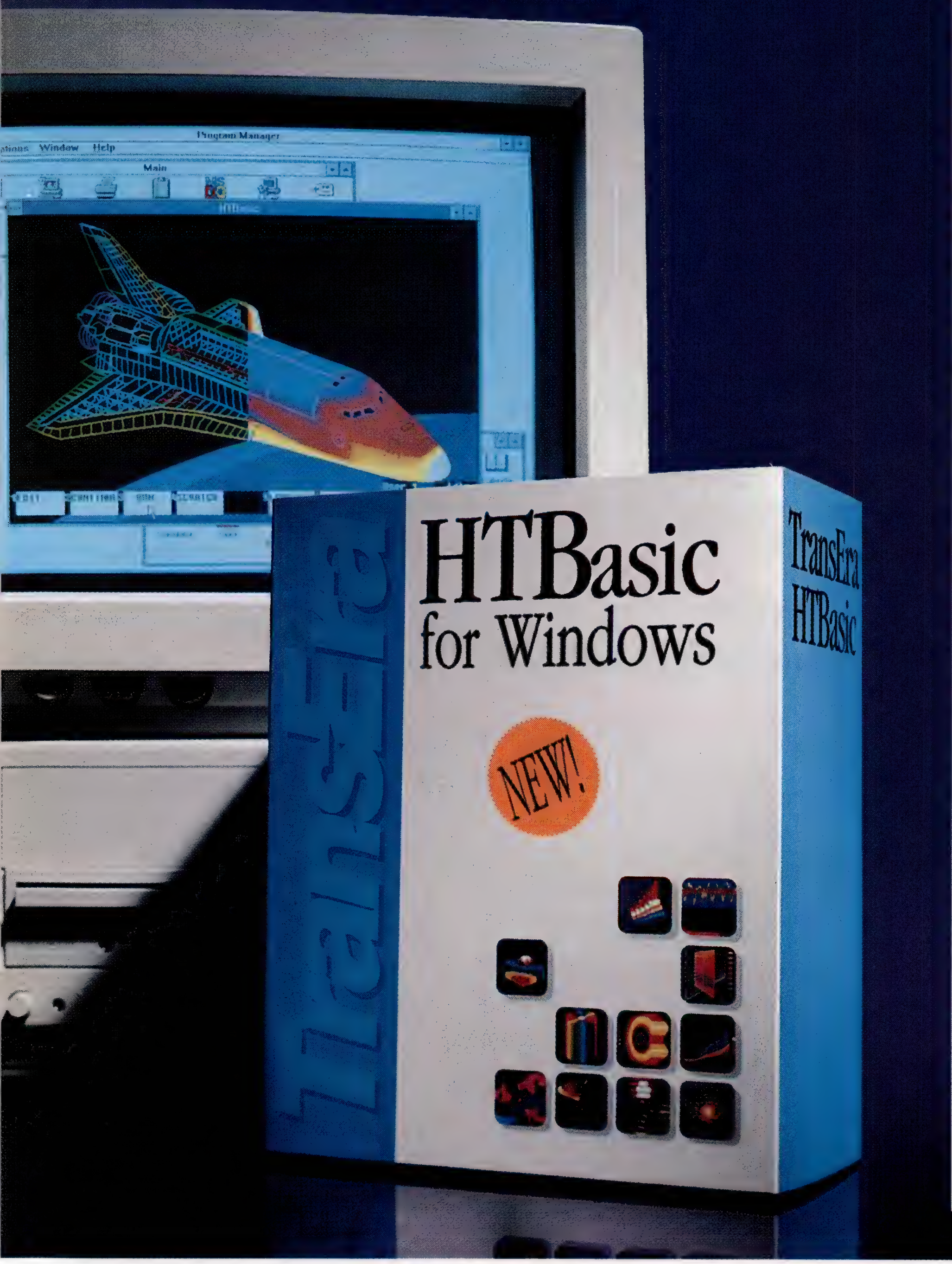
The power of HP BASIC
The ease of Windows



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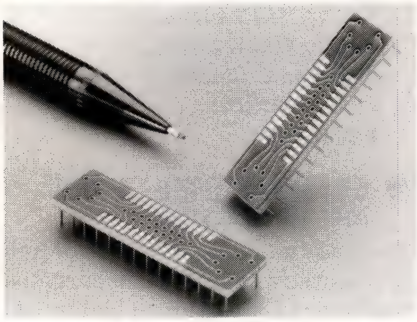
READER SERVICE 172

▼ SOIC-TO-DIP ADAPTER AVERTS PCB CHANGES

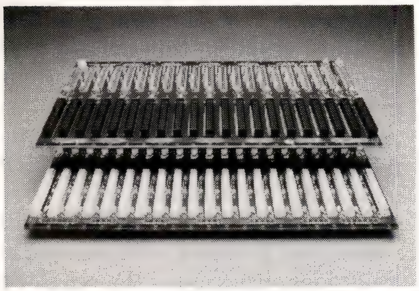
With Aries's SOIC-to-DIP adapter, designers can use a surface-mount, 28-pin small-outline IC within the confines of a traditional DIP layout without having to implement costly board-design changes. The adapter is a 0.300-in.-center, 0.100-in.-pitch DIP device with SMT pads on top to accept a 28-pin, 0.050-in.-pitch SOIC. Pins are tin/nickel-plated phosphor bronze. Pricing for a 28-350002-10 SOIC-to-DIP adapter is $4 in lots of 100. Delivery is from stock to three weeks.



Aries Electronics Inc.
P.O. Box 130
Frenchtown, NJ 08825
(908) 996-6841
▶CIRCLE 747

▼ VMEbus BACKPLANES AUTOMATE DAISY CHAINS

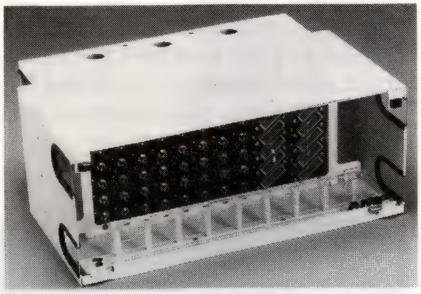
Optional automatic daisy-chain connections are now available in a line of monolithic VMEbus backplanes. The automatic jumpering is offered on the company's full range of backplane sizes, which run from two to 21 slots and are available off the shelf. The monolithic backplanes improve the performance and reliability of VMEbus systems by using a common J1/J2 substrate instead of a separate J1 upper portion and J2 lower portion of the backplane. This ensures that impedences are matched. The backplanes meet or exceed all requirements of the VME 64 standard, providing on-board termination and performance of better than 80 Mbytes/s. Call for pricing and delivery.



Dawn VME Products Inc.
47073 Warm Springs Blvd.
Fremont, CA 94539
(415) 657-4444
▶CIRCLE 748

▼ MODULAR UNIT MANAGES FIBERS

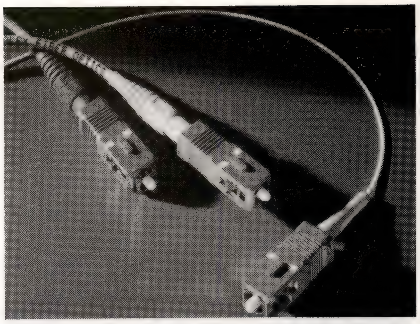
A versatile means of terminating and managing fiber-optic cables is embodied in AMP's termination and distribution unit (ATDU). The ATDU features modular construction and is well-suited for use in local-area networks, central-office networking, and telecommunication applications. The rack-mounted unit is designed to provide added cable protection for box-to-box routing while maintaining cables within the 17-in.-wide by 12-in.-deep enclosure. Standard features include universal mounting brackets for both 19- and 23-in. EIA and WECO racks, cable-routing rings, and removable front and rear access doors. Pricing depends on configuration and quantity. Delivery is in two weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶CIRCLE 749

▼ ONE-PIECE CONNECTOR CUTS INSTALLED COSTS

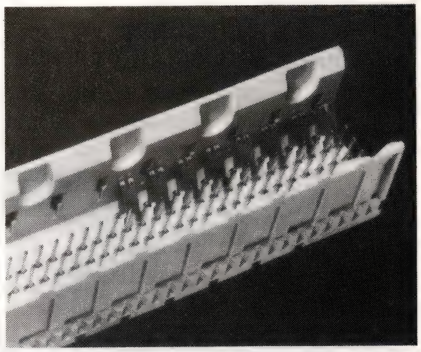
Total installation costs can be lessened by using Molex's one-piece SC/PC or SC/APC fiber-optic connectors. The SC one-piece-body connector is specially designed for distribution applications and meets Bellcore TR 326 Issue III specifications. Applications include local-area networks, CATV, active-device termination, and other network uses. The pre-assembled connector features a low insertion loss of 0.10 dB typical for single mode and a low return loss of less than 48 dB typical single-mode (super PC) and less than 55 dB typical single-mode (ultra PC). It's also offered in multi-mode versions. Pricing ranges from $4 to $15 depending on style and quantity.



Molex Fiber Optic
Interconnect Technologies Inc.
2111 Oxford Rd.
Des Plaines, IL 60018
(708) 803-3600
▶CIRCLE 750

▼ FUTUREBUS+ HEADER FEATURES SHUNTING

Mechanical shunts that electrically common up to 24 pairs of contacts is featured in the Z-Pack 2-mm Futurebus+ pin header. When unmated, the odd-even-position pins in Row A are shunted. When mated, the shunt contacts are deflected by the receptacle housing. The shunts can be selectively loaded and permit signal connection in the header without requring logic or an additional means of interconnection. Available in 24, 48, 96, and 192 positions, the shunted header uses a standard footprint to mate with standard receptacles and requires no added holes in the pc board. Pricing depends on specific signal and shunt configurations. Delivery is in eight weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶CIRCLE 751

▼ LED LAMPS, CAPS SUIT PANEL TASKS

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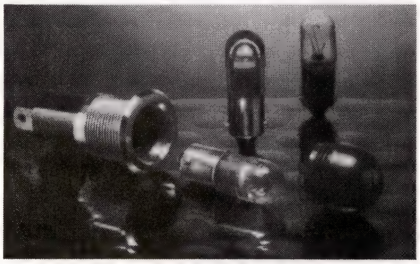

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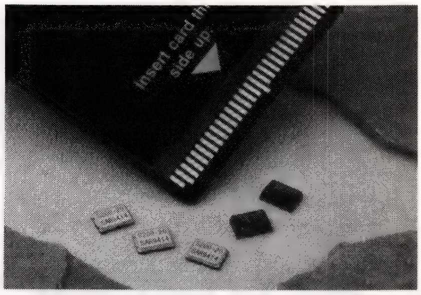

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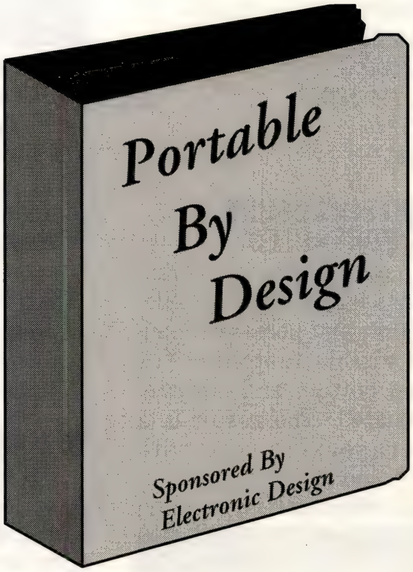

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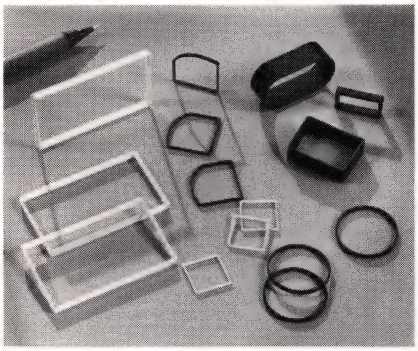

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▼ FASTENERS, INSERTS STRENGTHEN ASSEMBLIES

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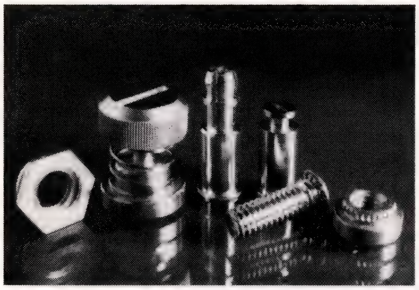

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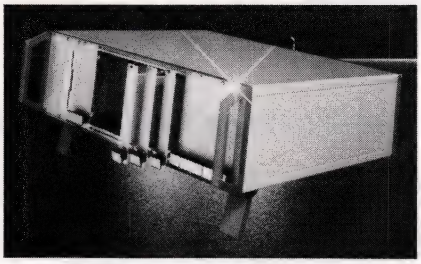

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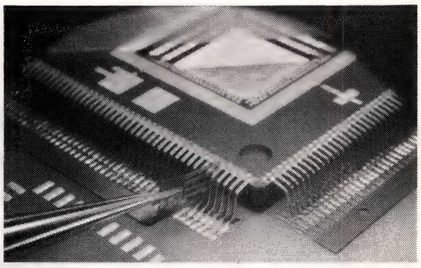

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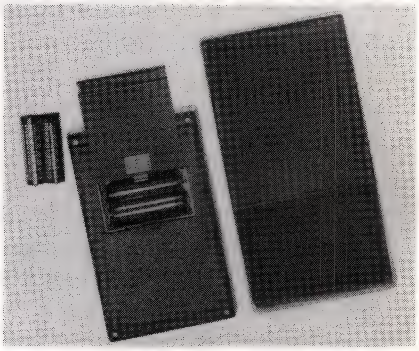

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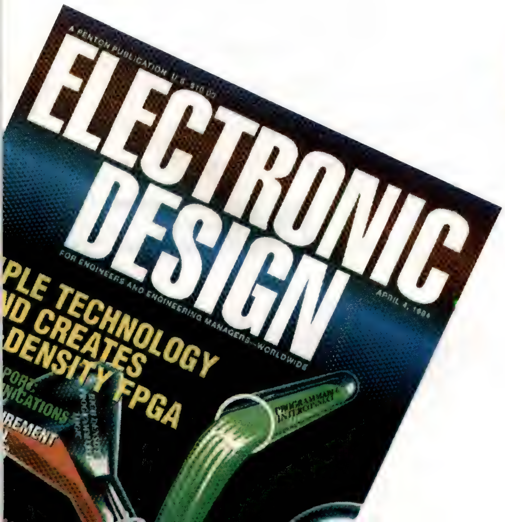

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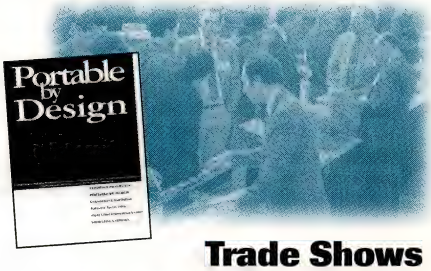

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READER SERVICE 157

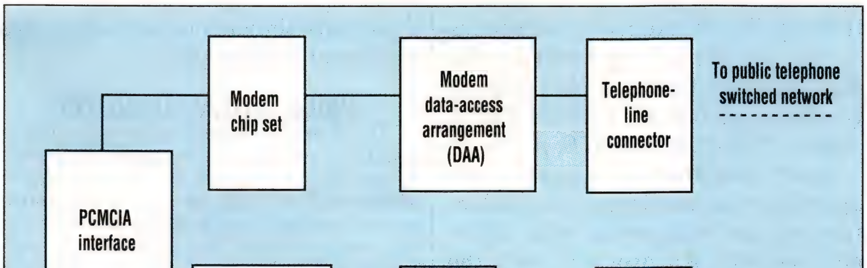
PCMCIA FAX-MODEM AND LAN RUN SIMULTANEOUSLY

TINY RJ-11/RJ-45 CONNECTION DEVICE USES STANDARD CABLES, ELIMINATES "DONGLE."

RICHARD NASS

One goal most PCMCIA card vendors are striving for is to combine the functionality of more than one device onto a single card. This is coveted particularly by many end users, who require more than one function yet have only one PCMCIA slot. The functions available today in a PCMCIA-card format include fax-modems, local-area-network (LAN) connections, rotating and solid-state mass storage, SCSI interfaces, sound cards, and so on. But in almost every case, each function resides in a card of its own.

Now, Apex Data Inc. has come up with an answer to the lack of multifunctionality by squeezing both a fax-modem and an Ethernet LAN onto one card. Dubbed the Combo, it holds a V.32bis modem that transfers data and facsimiles at 14.4 kbits/s. With V.42 data compression, speeds up to 57.6 kbits/s can be achieved. Throughput is further enhanced using an onboard 16C550 universal asynchronous receiver/transmitter (UART). Other components include a modem data-access-arrangement (DAA) unit and chip set, the PCMCIA interface, and the LAN medium interface and access controller *(Fig. 1)*. The Ethernet solution supports either 10Base-T or 10Base-2 installations.


Modem chip set
Modem data-access arrangement (DAA)
Telephone-line connector
To public telephone switched network
PCMCIA interface
Local-area-network (LAN) media-access control (MAC)
LAN medium interface
LAN connector
To LAN

1. THE BASIC COMPONENTS OF THE COMBO card designed by Apex Data include a modem data-access arrangement (DAA) and chip set, the PCMCIA interface, and the local-area-network (LAN) medium interface and access controller. The card offers simultaneous fax-modem and LAN functionality.

CLEAN AND EASY CONNECTION

What makes the Combo a unique solution is the connection scheme developed by Apex's engineers. Employing a device that's internally code-named Raider, users can insert an RJ-11 and a RJ-45 plug directly into the card at the same time. Raider is a device that's identical in width and height to the Type II PCMCIA card, and has a length of 0.75 in. It connects to the back of the Combo card and has two jacks, one for the telephone line (RJ-11) and the other for the Ethernet connection (RJ-45) *(Fig. 2)*.

When the plug is inserted into the receptacle, the upper edge of Raider expands and conforms around the plug. That's possible because it's manufactured using a technique called cold-molding, which attaches rubber to plastic. When the connector is removed from Raider, the device returns to its original shape.

Raider holds another advantage over other competitive connectors. When the Combo-Raider duo is plugged into the upper slot of a dual-slot system, the user still has complete access to the lower slot. Almost all other solutions employ a cable that attaches to a larger connector, called a "dongle." The dongle is a female receptacle for an RJ-11 or RJ-45 connector and an external DAA. One other technique accepts the RJ-11 plug in a vertical fashion, blocking the lower slot.

No special cables are required for either the LAN or modem connec-

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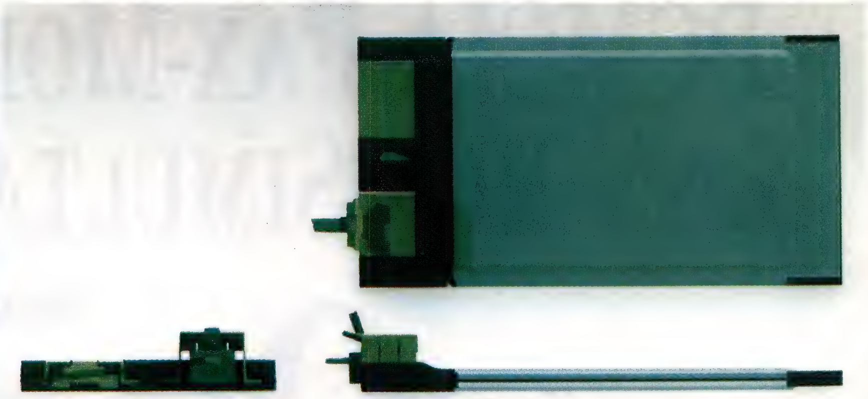

2. RAIDER'S UNIQUE CONNECTION SCHEME holds both an RJ-11 and an RJ-45 at the same time. Raider, developed by Apex Data, is the same width and height of a Type II PCMCIA card and has a length of 0.75 in. It connects to the back of the Combo card. When the jack holds a plug, Raider expands and conforms around the plug. In the figure, an RJ-11 is connected to Raider, while the RJ-45 socket is unoccupied.

tions when using Raider. "If a user loses or forgets to bring along the cable, a new one could be purchased at any electronics store for $2. Or they can just use the phone cable in a hotel room to access the modem," says John Chess, president of Apex Data.

Raider connects to Combo using a standard Honda 15-pin output connector, which is now specified by the PCMCIA standard. Without Raider, users still can attach their cables to the Combo card using a custom connector from Apex Data.

The Combo had to overcome a technical hurdle that's inherent to PCMCIA cards in general—there's only one interrupt signal between the card and the host computer. Therefore, designing a dual-function card required a way generate a second interrupt. The PCMCIA Committee is in the process of standardizing the dual-interrupt technique, but nothing is official yet *(see R. NASS'S TECH ANALYSIS: THIS ISSUE, p. 51)*.

Apex's designers developed three approaches to developing a second interrupt, and each works with different systems. All are built into the Combo, just implemented differently using a hardware-software scheme.

The first approach uses the battery-voltage-dead (BVD) or status-change signal, which notifies the PCMCIA controller when the voltage drops below a certain level. When the system needs the signal, the Apex software enablers take over. When the enabler has to take control, the card and socket services are circumvented.

The second approach is a shared interrupt. The card employs just the single interrupt pin and detects which device is causing the interrupt. This presents a problem because, based on how modems operate, detecting the interrupt could cause it to reset. The solution, therefore, is to poll for a LAN interrupt. If one occurs, it gets routed using a software interrupt. This technique is compatible with card and socket services.

The third approach employs a polling mode where the LAN polls for an interrupt while the modem gets a dedicated interrupt. This works well in Novell environments, but not as efficiently in Microsoft NDIS environments, particularly because NDIS requires its own dedicated interrupt. This scheme offers reasonable throughput, but it degrades performance slightly.

PRICE AND AVAILABILITY

The Combo multifunction fax-modem and LAN card is available now for $529 each. Large-volume discounts are available. Raider will be available later in the fourth quarter and will ship with the Combo card at no additional cost. Also, anyone who purchases a Combo card before the release of Raider will receive a free Raider when it becomes available.

Apex Data Inc., 6624 Owens Dr., Pleasanton, CA 94588; (800) 841-APEX or (510) 416-5656.
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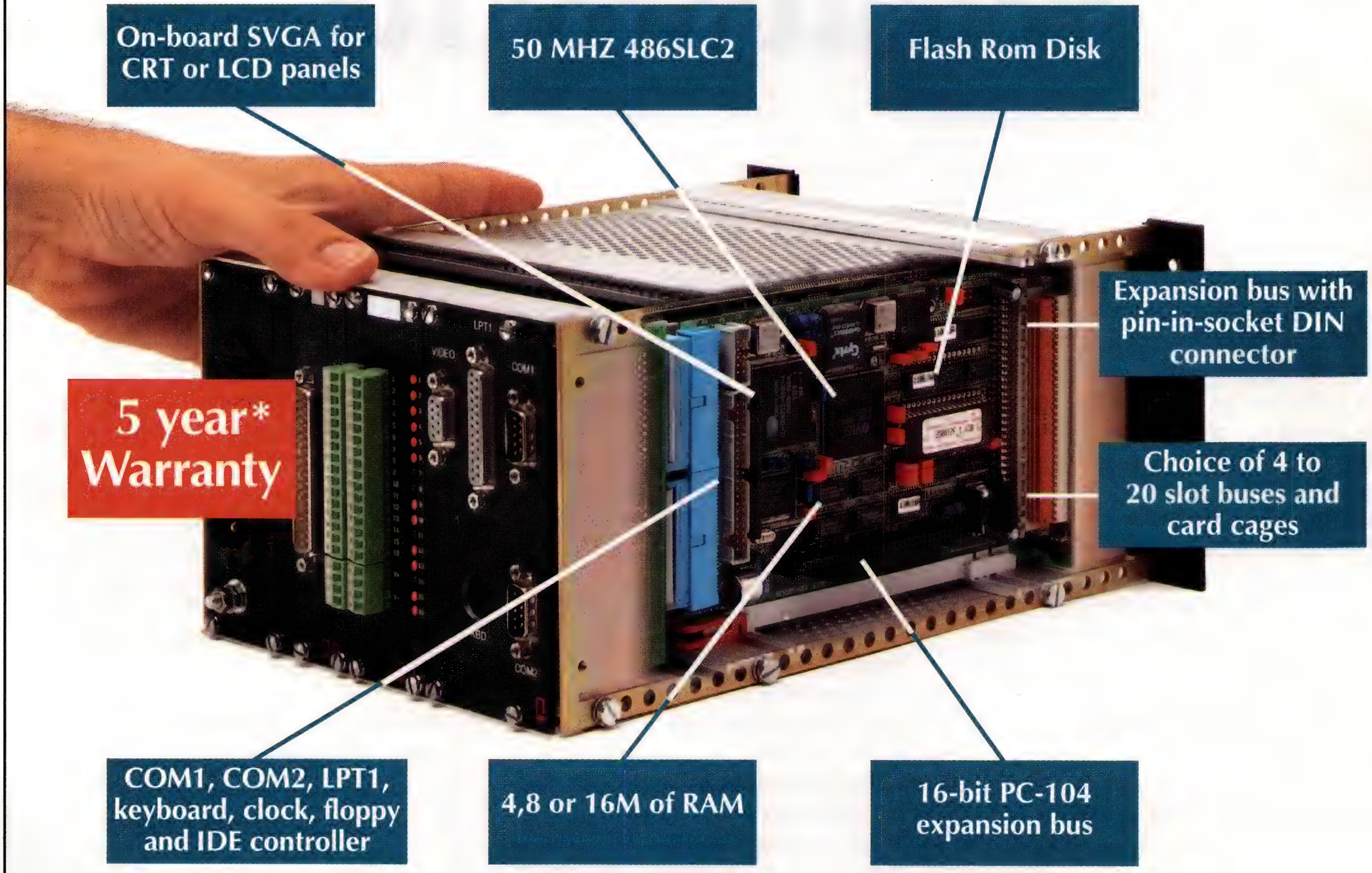
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CIRCLE 920

Active SCSI Terminator Works In 3.3-V Systems

A nine-line active SCSI terminator, the biCMOS-based UCC5614 can serve in systems that operate from power supplies that span 3.3 to 5.25 V. The terminator includes selectable 110-Ω and 2.5-kΩ termination modes and internal circuits that trim the output current to within a 4% tolerance level, maximizing signal integrity in Fast SCSI systems. To operate in 3.3-V systems, the UCC5614 incorporates a regulator with a 0.2-V dropout and a 2.7-V reference; for operation at 5.25 V, an additional terminal power source provides the higher voltage externally. With a 2-pF channel capacitance, the UCC5614 offers what Unitrode Integrated Circuits Corp., Merrimack, N.H., believes is the lowest channel capacitance in the industry. It also consumes very little current during disconnect (drawing just 1 mA). When used with short buses (less than 8 in.), such as in many portable systems, a low-power mode further reduces the current drain.

The terminator chip also includes a sink/source regulator that handles up to 300 mA—enough to permit the use of active-negation drivers. The UCC5614 is pin-compatible with other nine-line SCSI terminators from Unitrode and it allows hot-pluggable operation. In lots of 1000 units, the UCC5614 sells for $2.90 each, with production quantities in 16-lead DIPs, or 24- or 28-lead surface-mount packages, available immediately. Contact Rick DeMars, (603) 424-2410. *DB*

CIRCLE 921

Fast 3.3-V PLDs Offer No-Compromise Solution

Optimized to deliver propagation delays of as little as 15 ns, the GAL16LV8ZD and 20LV8ZD families of 20- and 28-pin programmable-logic circuits can operate from 3.3-V power supplies yet interface with either 3.3- or 5-V logic systems. The 3.3-V PLDs from Lattice Semiconductor Corp., Hillsboro, Ore., typically consume just 45 mA (55 mA maximum) from a 3.3-V supply—about half the current of 5-V devices—yet can operate at clock speeds of up to 62.5 MHz. When the system idles, a dedicated power-down pin lets the PLDs go into a sleep mode, where they draw just 50 μA. Production quantities of both 15- and 25-ns speed grades of the 20- and 28-pin PLDs are immediately available. In 1000-piece lots, the chips range from $2.25 each (for the 25-ns, 20-pin unit) to $4.90 (for the 15-ns, 28-lead GAL). Call Stan Kopec, (503) 681-0118. *DB*

CIRCLE 922

Gang Programmer Handles Dense Devices

The use of an independent socket structure allows the System General Multi-APRO gang programmer to accommodate increasingly dense memory products and smaller die sizes. The programmer will be able to handle 64-Mbit and beyond flash and EPROM devices without the problem of noise-related issues. Based on a 48-pin driver architecture, the programmer comes with one universal socket but can be expanded to as many as eight sockets. All types of packages are supported. It operates as a standalone unit or through a PC via an RS-232 interface. The Multi-APRO can program some devices that have lacked gang-programming support in the past, including Motorola's 711, 811, 705, and 708 microcontrollers, the Philips 87C75X, and the Intel 87C196 family of microcontrollers. Cabling and control software for the interface are supplied. Prices start at $1995. Contact Tim Morse at (408) 263-6667. *JN*

CIRCLE 923

Edited by Clifford Meth

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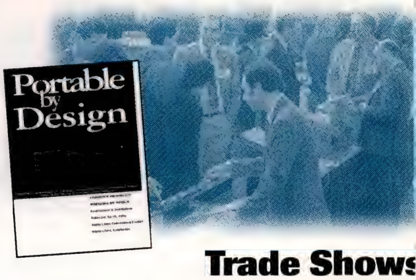

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USER-CONFIGURABLE FLASH MEMORY APPEARS AS BY-EIGHT OR BY-16 BITS

The first in a family of user-configurable flash-based nonvolatile memories, the Am29F400 allows designers to select the chip's I/O option via a control pin. Consequently, the 4-Mbit memory can appear as 512 kwords by 8 bits, or as 256 kwords by 16 bits. In either organization, the memory has access times of 70 to 150 ns, depending upon the speed grade.

The memory is subdivided into 11 unequal-sized sectors—one that holds 16 kbytes, two that hold 8 kbytes, one that holds 32 kbytes, and seven that each hold 64 kbytes. Sectors can be erased individually or in multiples (these features are similar to those in the Intel boot-block flash). Selected sectors can be hardware protected either individually, or in groups to prevent data corruption. However, a new function, "temporary sector unprotect," activated through the Reset pin, allows protected sectors to be temporarily unlocked. This permits in-system updates of protected data.

The smallest blocks—the boot sectors—are located at either the top or bottom of the address map (the 29F400T or 29F400B, respectively). That allows the memories to interface with CPUs that boot either from the low address or from the high address. The memory's internal state machine can suspend a write operation for the system to perform a read, and then continue the write once the read is finished. A Reset signal can terminate any operation and reset the internal state machine to the read mode in a maximum of 20 μs, so users can synchronize the memory to the host CPU.

The 29F400 needs a 5-V supply and draws just 25 μA on standby and 30 mA during write/erase. In addition to the 4-Mbit memory, which is now sampling, 1- and 2-Mbit versions will be released in the fourth quarter. The 120-ns Am29F400, housed in a 44-lead SO package, sells for $16 each in lots of 1000.

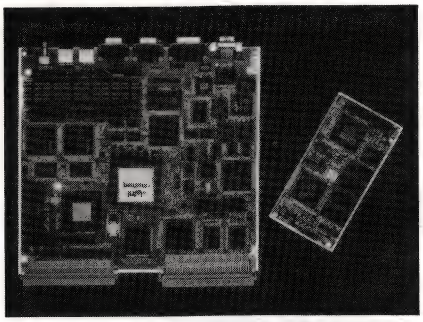
***Advanced Micro Devices Inc.**, One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453; (408) 732-2400.* CIRCLE 620

■ *DAVE BURSKY*

PENTIUM-BASED MULTIBUS II SBC TAKES ADVANTAGE OF PCI LOCAL BUS

Pentium microprocessors have made an impact in the PC market and are starting to displace the previous-generation 486 processors. Now, the high-performance CPUs are appearing on a Multibus II board. The single-board computer (SBC) holds a 90-MHz 64-bit CPU. In addition, performance is further increased using a PCI local bus to connect I/O devices.

A Multibus II-to-PCI bridge ASIC serves as the bus interface that electrically connects the Multibus II parallel system bus to the PCI bus. The PCI bus decouples the CPU and cache-memory controller from the I/O subsystem to supply an upgrade path.



The board can ship with a Super VGA accelerator module that plugs into the PCI bus. It's built with the ATI Mach64 graphics controller and 2 Mbytes of video RAM. The 64-bit module is compatible with such operating systems as DOS, Windows, Unix, and iRMX.

An IDE interface also connects to the PCI bus to increase hard-disk drive performance. Read-ahead and write buffers, combined with a 32-bit accelerated mode, minimize delays and maximize the utilization of the PCI and CPU buses.

The integrated SCSI-2 interface connects directly to the PCI bus using an Adaptec AIC-7850 controller chip. The SCSI connector is on the board's P2 connector. An AT/XT carrier can also be plugged into the P2 connector to accommodate the use of expansion cards. Front-panel connectors include two serial ports, one parallel port, the graphics connector, and keyboard and mouse connectors. An integrated Ethernet controller supplies 10-Mbit/s LAN connectivity. No jumpers or switches are needed for configuration, which is handled completely through software. The SBC also supports a remote boot capability.

The Pentium-based Multibus II SBC is available now for $6495. The graphics module costs an additional $599, both in single quantities.

***Intel Corp.**, 2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052; (800) 438-4769.* CIRCLE 621

■ *RICHARD NASS*

BYTE-WIDE SRAMS FOCUS ON LOW STANDBY DRAIN

With both a standard low-power standby mode and an ultra-low power version, the M5M51T08SL and 5408LL let designers keep the standby current levels to 2 μA, maximum, 50 nA, typical, with a 3-V supply, for the 128-kword by 8-bit M5M51T08, and to less then 10 μA, maximum, 400 nA typical, for the 512-kword by 8-bit version. Both SRAMs use thin-film transistor technology to form low-leakage six-transistor memory cells and also retain data with just a 2-V "keep-alive" power source. Options include versions that operate with access times of 55, 70, 100, or 120 ns. Both commercial- and industrial-temperature-range versions, housed in 32-lead type I TSOP and type II TSOP, are available for sampling. In lots of 10,000 units, the 1-Mbit version sells for $10.75 each, while the 4-Mbit version has a price tag of $96 in similar quantities. Call for delivery information. DB

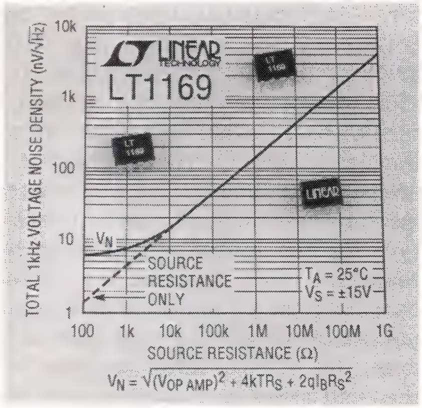
Mitsubishi Electronics America Inc., 1050 East Arques Ave., Sunnyvale, CA 94086; (408) 730-5900. CIRCLE 622

DUAL JFET OP AMP GUARANTEES 8 NV/$\sqrt{\text{HZ}}$ OF INPUT-VOLTAGE NOISE WITH A MINISCULE 10 PA OF BIAS CURRENT

Most low-bias-current JFET-input op amps sacrifice voltage noise for bias current. But the LT1169A, a dual JFET-input op amp, combines a maximum "warmed-up" bias current at 25°C ambient of just 10 pA with a maximum input voltage noise of 8 nV/$\sqrt{\text{Hz}}$.

The combination, a function of its patented "polygate" process technology and bias-current circuitry, represents an industry first. Voltage noise typically rises to 17 nV/$\sqrt{\text{Hz}}$ at 10 Hz, and 55 nV/$\sqrt{\text{Hz}}$ at 1 Hz. Essentially, the LT1169A runs 6 dB quieter than available low-input bias-current op amps. Low-frequency noise (1/f noise) typically runs less than 2 μV p-p in the band from 0.1 Hz to 10 Hz.

Unlike other JFET-input op amps, the input stage maintains its low input bias current over the full input common-mode-voltage (CMV) range of –11 V to +13.5 V (when running off split ±15-V rails). This results in an input impedance of 10^{13} Ω, and an input capacitance of just 1.5 pF over the full CMV. Such high-input impedance assures high-gain linearity when buffering high-source-impedance transducers.



The dual op amp provides system designers with another unique set of specifications. It guarantees a match of four parameters between the two devices on the die at 25°C, and over the commercial and the extended industrial temperature range. At 25°C, offset voltage matches within a maximum of 2.7 mV while noninverting bias current matches within a maximum of 8 pA. In addition, the devices' common-mode-rejection and power-supply-rejection ratios match within a minimum of 81 and 82 dB, respectively.

The matching specifications lend themselves to a number of applications, such as in the classic three-op-amp instrumentation amplifier (when low current and voltage noise are required), and as the input stage when amplifiers are paralleled to further reduce input-voltage noise. Other applications include photocurrent amplifiers; hydrophone amplifiers; high-sensitivity piezoelectric accelerometers; and very-low frequency, active RC filters.

The LT1169A is unconditionally stable, even when driving a 1000-pF capacitive load connected for a noise-gain of one—that is, as a unity-gain follower. As a result, it should perform well as an integrator and in a low-speed sample-and-hold amplifier. It slews at a minimum rate of 2.3 V/μs.

The low bias current (thus, low current noise) and low voltage noise suits these op amps for the T-network in the feedback loop of a current-to-voltage converter when sensing a few tens of picoamperes of current. The network can replace the noisy, high-resistance precision resistor with a quieter, lower-value, and often less expensive device. However, the circuit "noise gains" the op amp's input-voltage noise.

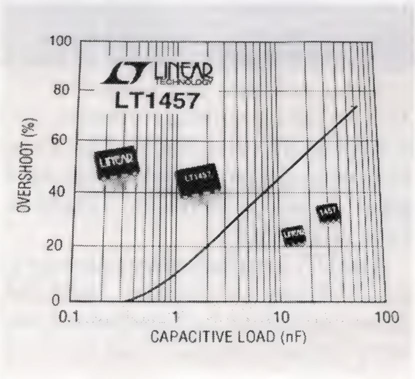
Other minimum/maximum specifications include an input-offset voltage of 1500 μV, an offset drift of 40 μV/°C, and an open-loop voltage gain of 115 dB while putting ±10 V across 1000 Ω. The premium LT1169A is accompanied by the LT1169, which offers slightly lower performance. Both devices come in 8-pin plastic DIPs and SOICs. Pricing in quantities of 1000 runs $3.80 each for the LT1169, and $4.51 for the LT1169A.

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 4-LINEAR.* **CIRCLE 623**

■ *FRANK GOODENOUGH*

JFET-INPUT OP AMP DRIVES 10,000-PF LOADS WITHOUT OSCILLATING

The LT1457, a dual JFET-input device, can drive a 10,000-pF load without oscillation. Such a load might be found at the input to a sample-and-hold amplifier, or a charge-redistribution (switched-capacitor) analog-to-digital converter. Other applications include photodiode amplifiers and voltage-to-frequency converters.



The JFET-input op amp also offers the industry's lowest maximum input-offset voltage for a dual JFET. It runs just 450 μV in an 8-pin DIP and 1200 μV in an 8-pin SOIC.

Offset-voltage drift, which is often more important than initial offset voltage, typically runs less than 4 μV/°C. Bias current, which approximately doubles every 10°C and is usually specified at 25°C, is specified at 70°C. It typically runs less than ±50 pA for all grades, and is guaranteed to be less than ±250 pA at that temperature for the ac grade. The op amp slews at 2 V/μs.

***Linear Technology Corp.**,1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott, (408) 432-1900.* **CIRCLE 624**

■ *FRANK GOODENOUGH*

MR HEADS PUSH DRIVE CAPACITY TO 2.2 GBYTES

By employing a 5400-rpm rotational speed, magneto-resistive (MR) heads, and banded recording, the Capella series of 1-in.-high 3.5-in. disk drives can store up to 2.2 Gbytes of data. This is combined with a host-user data-transfer rate of 7.5 Mbytes/s, an average seek time of 8 ms, and a track-to-track seek time of 1 ms. Other features of the SCSI-based drive include a 1-kbyte cache buffer, an embedded servo, and an optional write-back cache. In addition, another performance boost comes from a proprietary algorithm, called three-dimensional rotationally-optimized seek execution (3D ROSE), which reorders commands to minimize seek and rotational delay. The MR heads help raise the MTBF of the Capella series to 800,000 hours. Available sometime in the fourth quarter, the Capella 3221 2.2-Gbyte drive sells for $1720. Lower-capacity units are also available. RN

Avastor Inc., 333 South St., Shrewsbury, MA 01545; (800) DSP-DISK. **CIRCLE 625**

POWERBOOKS GAIN NEW OPTIONS

The latest generation of PowerBook portable computers offer a new interface design, multiple display options, a more intelligent and efficient battery technology, and increased expansion. The four models in the 500 series include the 520, 520c, 540, and 540c (the "c" designates a color display). Based on a Motorola 68LC040 microprocessor running at 50 or 66 MHz internally, the systems offer up to 36 Mbytes of system memory, and 320 Mbytes of hard-disk storage. The PowerBook's trackball has been replaced by a track-pad pointing device. With no moving parts, it offers a direct, reliable interface with accurate cursor control. For expansion, the systems include a PCMCIA slot. Built-in Ethernet offers a high-speed networking capability. And the nickel-metal-hydride batteries extend the life to seven hours. Prices range from $2269 to $5539. RN

Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014; (408) 996-1010. **CIRCLE 626**

VME64, PCI SERVER RUNS REAL-TIME UNIX

The ability to run real-time Unix is one of the features of the Linden AXP VMEbus SMP server. The Alpha system is based on VME64, with five available 6U slots. In addition, there are three available PCI slots that permit developers to do their own high-performance customization. Linden can hold up to four Alpha RISC CPUs and 2 Gbytes of system memory. Data is passed internally between memory and the processors over a 128-bit system bus. A bridge is used to connect to the PCI bus. Two packaging options are available, a tower model or a desktop configuration. Software support is available using OSF version 3.0 and OpenVMS AXP version 6.1. Applications for Linden include communications and medical imaging. Available now, prices start at $26,000. RN

Digital Equipment Corp., 1 Digital Dr., Merrimack, NH 03054; (800) DIGITAL. **CIRCLE 627**

X TERMINALS RUN WINDOWS AND MAC APPS

Support for MS Windows and Macintosh applications is included in the ViewStation Ultra series of X terminals. The terminals can also handle multimedia functions and PostScript display. The series is built an i960 processor to achieve a benchmark rating of 152,000 Xstones. PC-compatible floppy disks can be read to and written from, permitting users to transfer files or access PC applications locally. Running the files locally helps offload an existing host computer. Applications that are bundled include OSF/Motif and OpenLook, emulation of DEC VT320 and IBM 3270 terminals, a clock, a calculator, a screen saver, and a PostScript display application. Built-in PCMCIA slots offer instant upgradability. Prices go from $1699 to 3599. RN

Human Designed Systems Inc., 421 Feheley Dr., King of Prussia, PA 19406; (610) 277-8300. **CIRCLE 628**

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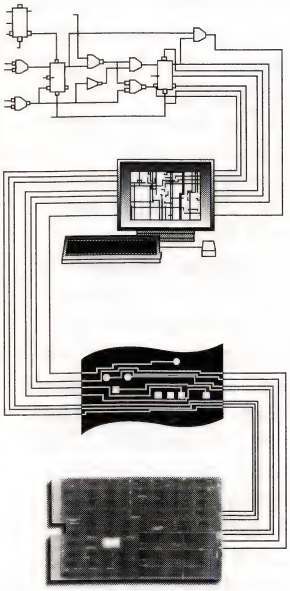

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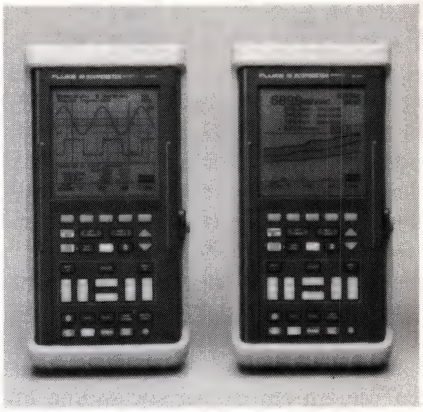
READER SERVICE 97

HANDHELD SCOPE-DMM MAKES AUTOMATED MEASUREMENTS

The ScopeMeter Series II combination digital oscilloscope and multimeter instruments offer a host of new features and measurement capabilities. Like the original ScopeMeter series, the new units combine a dual-channel, 50-MHz digital storage oscilloscope with a 3-2/3-digit true-rms multimeter in a battery-powered handheld instrument.

A Measure Menu offers direct access to up to 33 measurement tasks. The user picks the needed measurement from the menu and the instrument automatically configures itself for the measurement. Also, the newly added Continuous Autoset function dynamically monitors the input signals and continuously selects the correct time base, input range, trigger level, slope, and source as the user moves the probe from one test point to another.

Four versions are available. The Model 91 has one channel, 18 directly accessible measurements, and 18 meter measurements. The Model 92 adds a second channel. The two-channel Model 96 has 33 directly accessible measurements and 15 scope cursor measurements, five screen memories, 10 waveform memories, and 20 setup memories. Among other features, the two-channel Model 99 has additional memories and a signal generator that can produce sine and square waves and component test signals. It also adds waveform mathematics. All units come with a backlit display and a 600-V optically isolated RS-232C interface.



The Model 99 costs $2195, the Model 96 $1895, the Model 92 $1595, and the Model 91 $1295.

***Fluke Corp.**, P. O. Box 9090, Everett, WA 98206; (800) 443-5853.* CIRCLE 629

■ *JOHN NOVELLINO*

PORTABLE ATM ANALYZER HANDLES MULTIPLE INTERFACES

With the RC-200-C portable ATM protocol analyzer, users can test a variety of optical and coaxial interfaces simply by changing the instrument's interface card. The unit performs a wide range of tests, including AAL3/4 and AAL5 transmission and reception, statistics, decoding, and analysis.

Currently offered are four field-replaceable line interface units (LIUs) for bidirectional monitoring or one-channel simulation: a Sonet OC-3C/SDH STM-1 155-Mbit/s fiber interface, a DS-1/DS-3 coaxial interface, an E1/E3 coaxial interface, and a 100-Mbit/s TAXI fiber interface. Interface cards for other standards are scheduled for introduction in the near future.

The basic RC-200-C consists of a RISC-based unit with dual ATM segmentation and reassembly processors. This unit is controlled by the user's PC through Windows-based applications software for analysis, simulation, and statistical tasks.

The analyzer can simultaneously generate and monitor line traffic, including physical and data-link errors. Captured displays allow the user to analyze ATM data with detailed packet decoding. An optional software package permits IP encapsulation over ATM, as well as other LAN/WAN protocols. The unit is well suited for testing the upper layers of the OSI model.

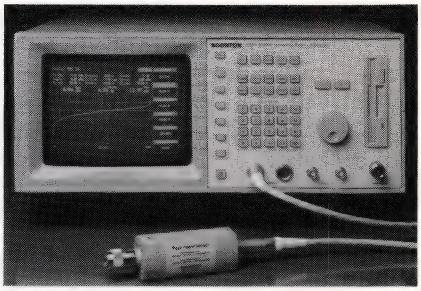
A basic RC-200-C with one LIU costs under $15,000. A system with three LIUs goes for under $25,000.

***RADCOM Equipment Inc.**, 900 Corporate Dr., Mahwah, NJ 07430; (201) 529-1100.* CIRCLE 630

■ *JOHN NOVELLINO*

POWER ANALYZER BOASTS 60-DB DYNAMIC RANGE

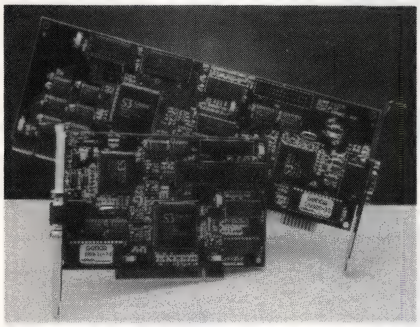
The Model 4500 digital-sampling power analyzer features a peak-power dynamic range of more than 60 dB, with a peak power sensor. The instrument offers statistical power measurement, plotting capability, and automatic measurements for precise analysis of digital communications products. Peak power range is –40 to +20 dB, and average power range is –50 to +20 dBm. Continuous power sampling can be done without a trigger event. All peak power readings can be normalized to average power in order to display a peak-to-average power-ratio curve. The unit makes seven automatic measurements in the statistical mode and 14 measurements in the pulse mode. The Model 4500 costs $15,000, with delivery in six to eight weeks. JN



Boonton Electronics Corp., 791 Route 10, Randolph, NJ 07869-1980; (201) 584-1077. CIRCLE 632

VIDEO ACCELERATOR HARNESSES S3 PROCESSOR

The Phantom 64 graphics accelerator is based on the S3 Vision864 chip, which is built with a 64-bit architecture. The board displays 24-bit color at 1280 by 1024 pixels and the maximum refresh rate is 106 Hz. Both VL-Bus and PCI versions are available, each with either 1 or 2 Mbytes DRAM. The Phantom 64 supports VESA's DPMS specification for low power. Software drivers are included for Windows, Windows NT, OS/2, SCO Unix, AutoCAD, AutoShade, and 3-D-Studio. The 1-Mbyte board sells for $249, while the 2-Mbyte version is priced at $319. Both are available now. RN



Genoa Systems Corp., 75 East Trimble Rd., San Jose, CA 95131; (408) 432-9090. **CIRCLE 633**

REFERENCE KIT AIDS MULTIMEDIA DESIGNS

The Quantumdsp reference design package is a comprehensive set of design and manufacturing tools for developing ISA-bus multimedia cards based on the AT&T DSP3210 digital-signal processor. The kit lets designers quickly bring to market cards capable of handling several functions, including fax, modem, CD-quality stereo, and audio and video compression. The 27.5-MFLOPS DSP chip runs AT&T's Visible Caching Operating System (VCOS), which combines multitasking and compute-intensive application development with a modular set of tools. The kit also comes with a series of source files to implement the multimedia capabilities. Available now, the design kit sells for $25,000. RN

Communication Automation & Control Inc., 1642 Union Blvd., Suite 200, Allentown, PA 18103; (800) 367-6735 or (610) 776-6669. **CIRCLE 634**

ALPHA BOARD EXECUTES 333 MIPS

Running at peak frequency of 166 MHz, the ADD66-100 processor board can execute 333 MIPS and 166 MFLOPS. The board is based on a DEC Alpha AXP RISC microprocessor. It holds from 8 to 64 Mbytes of DRAM and up to 1 Mbyte of 15-ns cache memory. The ADD66-100 can be connected to other processor boards through four serial-communication links. It also supports ISA and PCI interfaces for peripheral connection. Suitable applications include image processing, fluid dynamics, and financial modeling. The CPU board can be employed either as an add-in processor or as a building block for a parallel-processor network. Software support is available using the DEC ANSI C compiler or the 3L parallel C compiler. RN

Advanced Computing Solutions, 5651 South West Arctic Dr., Beaverton, OR 97005; (503) 626-3896. **CIRCLE 635**

BOARD OFFERS 40-MHZ PIPELINED ARCHITECTURE

VMEbus workstations and PCs built with a VL-Bus local bus can benefit from the Modular Vision Computer (MVC), a scalable and configurable vision system. Driven by a 40-MHz pipelined architecture, the MVC 150/40 can process a 512- by 512-pixel image in less than 7.5 ms.

Suitable applications for the MVC include industrial machine vision, aerospace and defense-system development, and advanced scientific and medical image analysis. Up to 15 acquisition, processing, or I/O modules can be added as the application needs change or grow. Most standard cameras can be connected directly to the board. Included development software eases application integration. Prices for the vision-system board start at $7500 when purchased in large quantities. RN

Imaging Technology Inc., 55 Middlesex Tpke, Bedford, MA 01730; (617) 275-2700. **CIRCLE 636**

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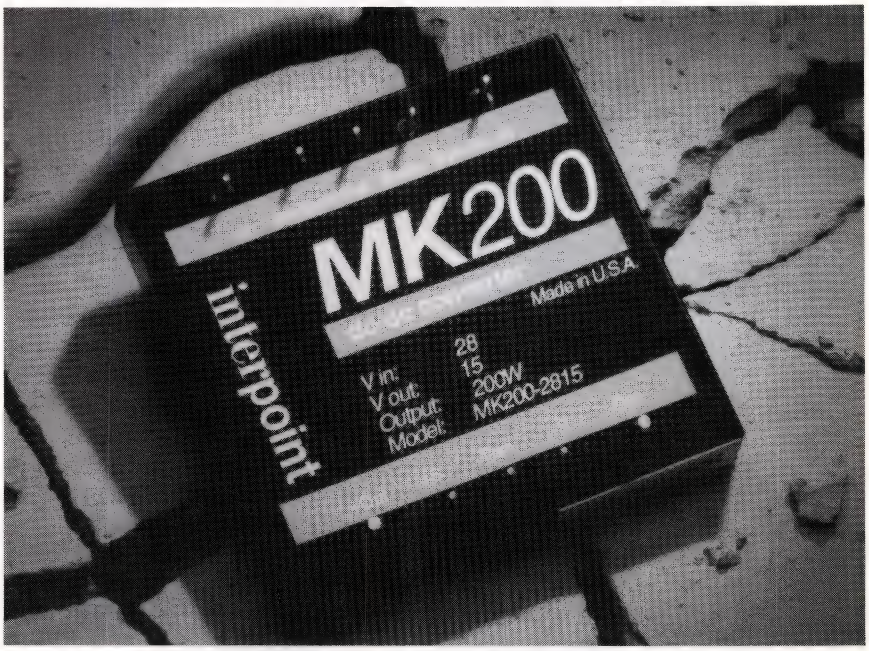


The claim of first standard dc-dc converter to provide 80 W/in.^{3} of usable power has been staked by Interpoint for its MK200 converter. Up to 200 W of output power are generated from within the unit's standard half-size case (2.4 by 2.28 by 0.45 in.). It's specifically designed to simplify the job of using converters by reducing or eliminating the need for external components.

To use most high-density converters, designers must add external capacitors to provide stable operation, build or buy bulky external input and output noise filters, attach large external heat sinks, and work around restricted input-voltage ranges. If the application calls for multiple outputs or for current sharing, multiple units must be connected with additional external components.

The MK200 converter simplifies the design of power systems by addressing these issues inside the converter's package. To start with, the unit is a fixed-frequency (1.2-MHz) forward converter with an industry-standard size and pinout. Its internal filter networks provide stable operation over all rated loading conditions with no external capacitors.

Power increases in the MK200 converter are achieved by applying the company's asymmetrical power-transfer (APT) technology to a surface-mount device. APT increases power density by using self-resetting magnetics and by allowing the converter's duty cycle to be extended beyond 50%, thereby both reducing losses and lowering the stress levels on key components. In the MK200 design, duty cycles approach 80%. In addition, a proprietary, lossless snubber design converts parasitic losses into usable power.

Noise levels are low enough (input ripple of 5 mA and output ripple of 5 mV) that in most applications, there's no need for external filtering—even in extremely noise-sensitive analog applications. Achieving such low noise levels required an untraditional approach to noise control.

Rather than concentrating on filtering, Interpoint's engineers designed a less noisy converter. The converter's integrated, planar transformers create half the switching noise of typical transformers. That's accomplished through use of multifunctional, epoxy-impregnated insulation materials with extremely low dielectric constants that yield capacitance across the isolation barrier of less than 20 pF.

These inherently low-noise magnetics are then applied to a dual-phase, phase-shifted topology in which the two phases are precisely offset to provide optimal noise cancellation. The result is that less than half the noise is generated as when conventional techniques and materials are used, even at high frequencies of up to 20 MHz, where effective filtering is a challenge.

The converter reduces or eliminates heat-sink needs by providing operating efficiencies of up to 90% and a full-power temperature rating of 125°C. In addition, it provides a full 2:1 or 2.5:1 input-voltage range to meet a wide variety of power-line limits. The first product offerings are 28-V dc nominal models rated for either 18 to 40 V or 16 to 40 V dc.

Both single- and dual-output models are offered as standard types. Single-output units share current with 95% accuracy over all load conditions without any external components. Other standard features include over-current protection, continous short-circuit protection, remote sense, output-voltage trim, high isolation (1500 V dc), and synchronization of switching frequency to an external clock.

Packaging is in a six-sided, sealed metal enclosure. All active silicon components are mounted on multichip modules for density and protection. Two versions of the converter will be available. In the high-reliability version, the MCMs are housed in a hermetically sealed ceramic leadless chip carrier produced on the company's MIL-STD-1772 assembly line. The commercial version will have the same environmental ratings and metal case, but will house the internal silicon in plastic LCCs.

The MK200 dc-dc converter will be available in January of 1995. Pricing for a hermetic, aerospace-grade unit will be $590 in OEM quantities.

Interpoint Corp., 10301 Willows Rd., P.O. Box 97005, Redmond, WA 98073-9705; (206) 882-3100.

CIRCLE 637

SINGLE-CHIP ENGINE CRUNCHES DES CYPHERS AT 240 MBITS/S

With the advent of client/server networks, distributed computing, and remote data-access, there has been an increasing demand for communication products that incorporate data-security features. One solution is a single-chip encrypt/decrypt chip that supports full-duplex digital-encrypted communications at up to 284 Mbits/s. The ROADRunner284 can be used to provide security for Internet communications, interactive multimedia networks, and both wired and wireless digital-packet communications as well as storage applications.

Implimented in 0.8-μm CMOS, the ROADRunner284 secures any serial bit-stream using the data encryption system (DES) algorithm and a 512-bit encryption key. Its unique architecture includes two separate DES engines and a third RISC-based controller, which allows for full-duplex, real-time communications even at it's maximum 284Mbit/s transmission rate. An on-chip RAM and user-definable ROM allow storage of the encryption key and other optional operating parameters.

An internal 512-by-16 FIFO buffer allows the encryption processors to handle "bursty" traffic at up to 640 Mbits/s. Additional FIFO buffers may be directly interfaced to either channel to provide deeper buffers if required.

The simplified high-speed digitalinterface and dual DMA controllers lend themselves to a variety of applications, including secure modem devices, encrypted LAN and WAN systems, encrypting network adapter cards, and secure wireless-communications devices. The chips may also find homes in multimedia consumer items, such as set-top boxes.

At its full clock speed of 40 MHz, the ROADRunner284 draws 7.5 W of 5-V power. For portable or low-power applications, an 8-MHz clock may be used to drop power draw to 1.5 while still processing data at speeds of up to 36 Mbits/s.

Priced at $75 in lots of 10,000 units, the ROADRunner is immediately available.

***Semaphore Communications Corp.**, 2040 Martin Ave., Santa Clara, CA, 95050; (408) 980-7750, fax -7769.* CIRCLE 638

■ *LEE GOLDBERG*

ASYNCH PORT BOOSTS SYSTEM PERFORMANCE

The TL16PC564APZ serial communications chip is designed specifically to boost the performance and lower the cost of PCMCIA applications in laptops, palmtops, faxes, and modems. The TL16PC564APZ combines a TL16C550 UART and all of the logic required to interface it directly with a PCMCIA bus. The chip's 64-byte transmit buffer greatly reduces the number of interrupts a host processor must deal with while transmitting data, freeing many processor cycles for other important tasks. The PCMCIA interface is fully compliant with the 2.01 standards and contains a 256-byte card-information structure, and an 8-byte configuration register. A bus-oriented interface is also included to facilitate connections with on-card microcontrollers. A single pin can be tied high or low to select either a separate address and data bus arrangement used by Motorola and TI processors, or a multiplexed bus/data scheme employed by most Intel and Zilog products. Available immediately, the TI16PC564APZ is housed in a 100-pin TQFP. Prcing for the device is $11.20 in lots of 1000. LG

Texas Instruments, Literature Response Center, SC-94077, PO Box 172228, Denver, CO, 80217; (800) 477-8924, ext 4500. CIRCLE 639

MODULAR OPTICAL TRANSCEIVERS

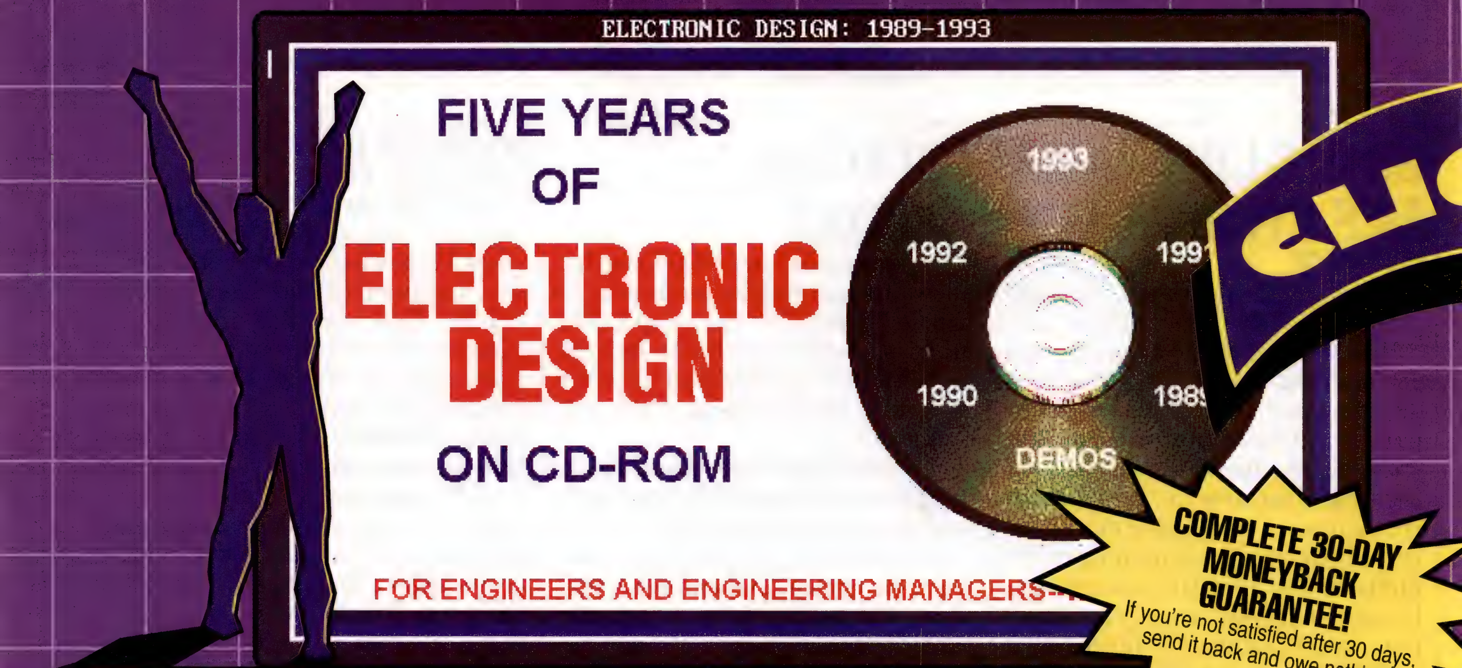
The HGLM series of optical interface modules are complete FC-0 compliant Fibre Channel links packaged in a standard GBaud Link Module (GLM). The modules integrate, transmit, and receive optics, drivers, clock, and data recovery, as well as serializer, deserializer, and laser-safety features. The optical interface is accomplished via standard dual SC receptacles. Optional high-speed electrical I/O connections are also included. The HGLM-0531 module provides a 531-Mbits/s data rate, while the HGLM-1063 module supports a 1063-Mbits/s rate. Both units run off of a single +5 V supply and accept 8b/10b encoded data inputs. Priced at $350 in lots of 1000, both units are available immediately. LG

Hewlett Packard Company, 5301 Stevens Creek Blvd., Santa Clara, CA 95052-8059; (800) 357-7715, ext. 8364. CIRCLE 640

FOUR-CHANNEL CODEC/ FILTER FOR PBX

The size and cost of PBX and central-office-to-network equipment is expected to shrink again with the introduction of the PEB 2465H, integrated four-channel codec/filter chip. Providing complete a-d and d-a functions for four speech channels, the codec contains all of the circuitry required for translating each channel between an analog signal and telephone network standard pulse-code modulation (PCM). The PEB 2465H uses programmable DSP technology instead of switched capacitors to accomplish it's conversions, making it easier to adapt to different environments. The programmable filters allow the chip to perform impedance matching for echo minimization, transhybrid balancing, and programming of filter functions to match nearly any global telephone-interface standard. With samples ready now, the PEB2465H will be available in production quantities by third quarter 1994. Pricing for the device is anticipated to be $12.70 in lots of 10,000. LG

Siemens Components Inc., 10950 North Tantau Ave., Cupertino, CA., 95014; (800) 777-4363, ext. 274. CIRCLE 641



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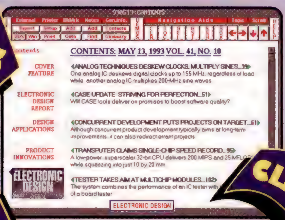

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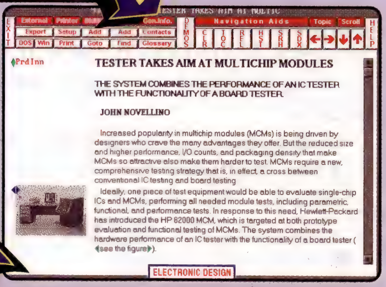
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ELECTRONIC DESIGN

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure).

THE HP 82000 MCM IS AVAILABLE with 50-, 100-, and 200-MHz ve channels and features an edge-placement accuracy of +/-250 ps

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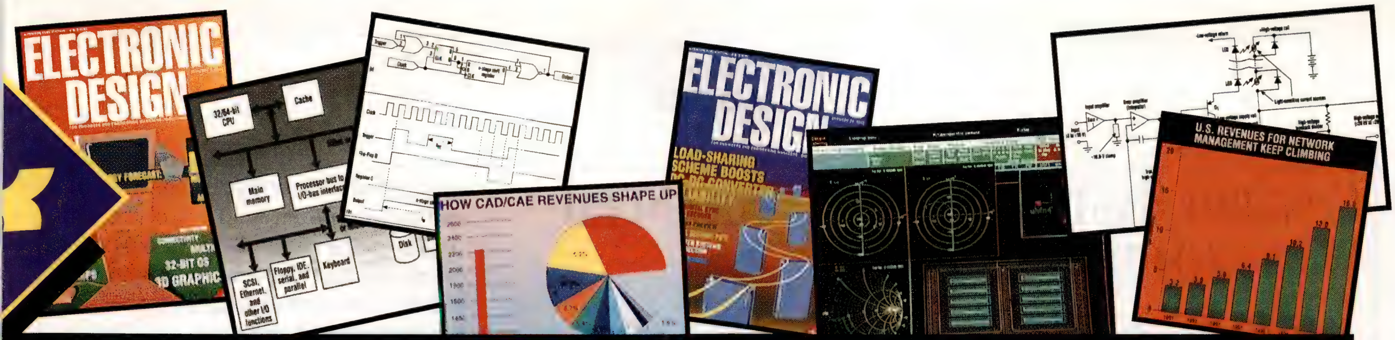
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HOW CAD/CAE REVENUES SHAPE UP
U.S. REVENUES FOR NETWORK MANAGEMENT KEEP CLIMBING
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Main memory
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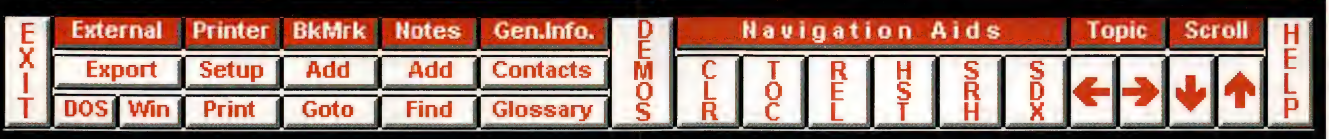
Floppy, IDE, serial, and parallel
Keyboard
32-BIT OS
3D GRAPHIC



Learn the backbone of the Electronic Design Magazine CD-ROM interface - the BUTTONBAR.

Powerful, hypertext-based commands let you quickly and efficiently find, re-find, link, make notations, leave bookmarks, export, print, search, get product demos, and even return to your operating system!

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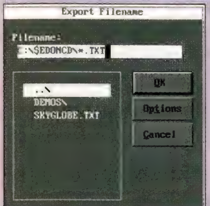

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DEMOS\
SKYGLOBE.TXT
```

The **Export** button will export any or all of an article based on your selection.

DOS & Win

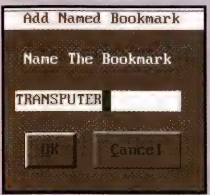
DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. These buttons make it easy for you to return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands

Setup & Print - This feature allows you to print articles, editorials, glossaries, illustrations, and even photos *(if your printer is capable)* directly from this CD. Great source for reference.

Bookmarks and Notes

BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. Mark a spot, and the bookmark is stored even if you quit.



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Add Named Bookmark
Name The Bookmark
TRANSPUTER
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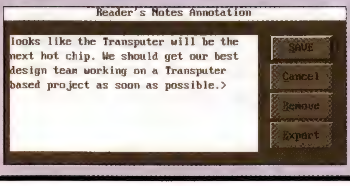
GOTO brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.



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Reader's Notes Annotation
looks like the Transputer will be the
next hot chip. We should get our best
design team working on a Transputer
based project as soon as possible.>
```

Gen. Info - Complete reference

Contacts - Company names, addresses, contact names, phone numbers- all of the information you need to follow up.

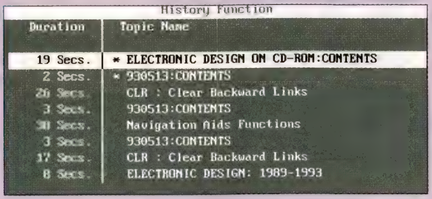
Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

Navigation Aids - Magellan you're not, and you don't need to be!

All the aids you'll need to motor your way through this CD in no time flat.

CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.



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                    History Function
 Duration   Topic Name

 19 Secs.   * ELECTRONIC DESIGN ON CD-ROM:CONTENTS
  2 Secs.   * 930513:CONTENTS
 26 Secs.     CLR : Clear Backward Links
  3 Secs.     930513:CONTENTS
 30 Secs.     Navigation Aids Functions
  3 Secs.     930513:CONTENTS
 17 Secs.     CLR : Clear Backward Links
  8 Secs.     ELECTRONIC DESIGN: 1989-1993
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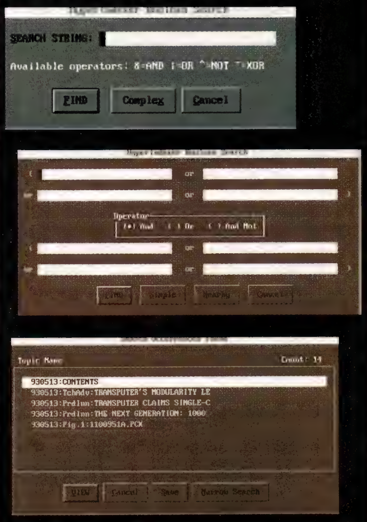
REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.

SEARCH dialog boxes

Simple search (top), Complex Search (center), and Search occurances found (bottom).



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SEARCH STRING:
Available operators: &=AND |=OR ^=NOT ~=XOR
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Topic Name                               Count: 14
 930513:CONTENTS
 930513:TchAdv:TRANSPUTER'S MODULARITY LE
 930513:PrdInn:TRANSPUTER CLAIMS SINGLE-C
 930513:PrdInn:THE NEXT GENERATION: 1000
 930513:Fig.1:1100951A.PCX
```

SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

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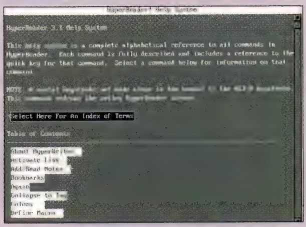

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is a complete alphabetical reference to all commands in
HyperReader.  Each command is fully described and includes a reference to the
quick key for that command.  Select a command below for information on that

Select Here For An Index of Terms

Add Read Notes
Bookmarks
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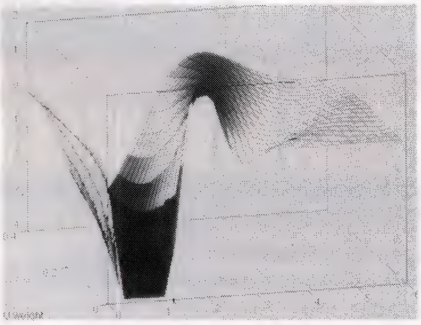
MINIMUM SYSTEM REQUIREMENTS

- ☞ 80386 PC or better
- ☞ VGA video card adaptor w/640 x 480 pixel resolution 16 colors.
- ☞ 1 meg ram
- ☞ MS-DOS Version 3.1 or later

CONTROL SYSTEM TOOLBOX ENHANCED WITH SIMULATION TOOLS



From The MathWorks, the Model Predictive Control Toolbox, the Frequency Domain System Identification Toolbox, and Simulink 1.3, extend the Matlab Technical Computing Environment with tools for modeling, simulating, and designing control systems. The Model Predictive Control Toolbox implements model predictive control techniques applied in process industries, aerospace, automotive, and other advanced control applications.

The Frequency Domain System Identification Toolbox contains specialized tools for creating a model of a linear dynamic system from measurements of its excitation and frequency response. Simulink 1.3 features new blocks, modeling tools, and visualization aids that make it easier to simulate complex systems and understand system behavior.

The Model Predictive Control Toolbox is used in the design of control strategies for scenarios where there are many variables, constraints on inputs and outputs, changing control objectives and/or equipment failure, and time delays. Some application design examples include engine speed control in the automotive industry, catalytic system control in petrochemical processing, and flow control in the pulp and paper industry. The toolbox includes more than 50 Matlab M-files for modeling, identification, and validation of multivariable systems and for controller design and simulation, system analysis, model building, and model conversions.

Simulink 1.3 helps engineers and scientists build, simulate and refine complex system models by providing more sophisticated and rigorous modeling and new simulation techniques. This new version introduces vectorized blocks and connections, wide vector lines, and scalar expansion of inputs and parameters—features that both simplify the layout of complicated system diagrams and make them easier to understand. New visualization techniques include sample-time coloration that graphically simulates different parts of a system operating at multiple sampling rates.

Simulink 1.3 also includes an enhanced block library, totaling over 80 blocks. New blocks include hit-crossing and logical operator blocks, making it easy to model systems that can drastically change behavior depending on internal or external conditions. Blocks are also included to tie Simulink to various Matlab toolboxes, including the popular Neural Network Toolbox.

Pricing for the Model Predictive Control Toolbox begins at $895 for MS-Windows and Macintosh; the Frequency-Domain System Identification Toolbox prices start at $395 for MS-Windows and Macintosh. The Model Predictive Control Toolbox and Frequency-Domain System Identification Toolbox both require Matlab 4.0 and are shipping on all Matlab 4.0 platforms.

Pricing for Simulink 1.3 begins at $1,995 for MS-Windows and Macintosh. It requires Matlab 4.2 and is shipping on PCs running MS-Windows, Macs, Sun Sparcstations, and Hewlett-Packard Series 700 workstations. Quantity and education discounts are available.

***The MathWorks Inc.**, 24 Prime Park Way, Natick, MA 01760; (508) 653-1415; fax -2997; e-mail:info@mathworks.com.*

CIRCLE 642

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DISK HELPS CREATE DATA-ACQUISITION SYSTEM

The DAQ Designer interactive data-acquisition planner has been updated to include a number of new products. The disk-based software from National Instruments, Austin, Texas, helps users configure systems for PC/XT/AT/EISA and Micro Channel-based computers. Through its graphical interface, DAQ Designer asks the developer questions about system requirements, such as the type and number of analog and digital signals, the type and number of sensors and signals, and signal conditioning needs. The program analyzes the answers and recommends specific plug-in boards, conditioning products, cable assemblies, and software packages. After the user has selected the products, DAQ Designer creates a summary list that can be stored or printed. JN **CIRCLE 941**

FILM RESISTORS IN VARIED ASSORTMENT

With 32 pages of engineering information and technical detail, a film-resistor catalog from Caddock Electronics Inc., Riverside, Calif., provides a valuable resource for designers. The complete scoop on a wide assortment of resistive elements is served up with tables of characteristics, descriptions, photographs, derating curves, and dimensional drawings. Included are high-voltage types, precision resistors, decade resistors, voltage dividers, shunts, resistor networks, power resistors, and more. DM **CIRCLE 942**

RELAY DATA BOOK BRIMS WITH DETAIL

With over 430 pages, the Relay Technical Data Book from Aromat Corp., New Providence, N.J., is a valuable resource to any designer. This full-line catalog provides complete information on hundreds of relays of all kinds, including reeds, SSRs, optically isolated types, power relays, and more. A section of general technical information includes definitions of relay terms, diagrams of relay construction, general application guidelines, process information, and more. Products are described in detail with tables of specs. DM

CIRCLE 943

BOARD RIGIDIZERS FEATURED IN BROCHURE

Detailed descriptions of various problem-solution situations dealing with board rigidizers and power-distribution issues are contained within a two-page brochure from Circuit Components Inc., Tempe, Ariz. Each case shows how designers used board stiffeners and bus bars to resolve problems related to pc-board warpage, power-distribution problems stemming from space constraints, and solder-joint cracking caused by excess vibration. DM

CIRCLE 944

BROCHURE AIDS BUILDERS OF VXIBUS SYSTEMS

A brochure from the VXIplug&play Alliance, Austin, Texas, contains information on standard frameworks, instrument drivers, soft front panels, and technical support that can help end users develop VXIbus systems. The four-page, four-color brochure discusses system-level issues, such as software, that are not standardized by the baseline VXIbus specification. Then the publication goes on to explain how to build VXIbus systems based on the frameworks endorsed by the VXIplug&play Alliance: DOS, Windows, and graphical Windows. The free brochure shows how to select a suitable framework and use it to guide the choice of VXIplug&play-compatible components. The VXIplug&play Alliance was formed to deal with issues beyond the scope of the VXIbus Consortium that affect the integration of multivendor VXIbus systems. JN

CIRCLE 945

WORLD-POWER GUIDE UPDATES EXPORTERS

The line power available in countries around the world is listed in the Current Guide for World Power, a 34-page booklet from California Instruments, San Diego, Calif., that helps in correct testing of products for export. The guide illustrates the types of electric plugs for domestic and commercial use in most countries and lists each country's type and frequency of current, number of phases, nominal voltage, and number of wires. It also indicates whether the power is stable enough for electric clocks. Variances in major cities are also accounted for. A brief introduction highlights the company's single- and three-phase precision ac-power products. DM

CIRCLE 946

INTERFACE PANELS CAPABILITIES OUTLINED

In a color brochure, Cherry Electrical Products, Waukegan, Ill., outlines its capabilities in designing electronic interface panels. These man-to-machine interfaces can make or break an end product. The brochure explains Cherry's expertise in designing and assembling interface panels that can make a difference. Sections cover customized panel design, advanced manufacturing, quality issues, and the company's worldwide resources. DM **CIRCLE 947**

MILLIONS OF OPTIONS FILL SWITCH CATALOG

Thanks to the Build-A-Switch format, Catalog No. 9308 from C&K Components Inc., Newton, Mass., gives users the opportunity to design their own application-specific switches from millions of possible combinations. The 325-page catalog details a variety of switch types, including miniature, subminiature, and ultra-miniature toggles, rockers, lever handles, slides, rotaries, dual in-line packages, coded types, pushbuttons, piezoelectric, SMT, and process-compatible types. Complete specifications, including electrical and mechanical ratings and agency approvals, are provided. DM

CIRCLE 948

RF TASKS NOTED FOR 3-MM SWITCHES

A four-page application note from Bourns Inc., Trimpot Div., Riverside, Calif., describes how a 3-mm, SPDT rotary switch can be put to advantage in the design of RF circuitry. With numerous charts and graphs as well as a well-written short essay, it's shown how the model 7813 rotary switch can be used in RF circuits without causing signal distortion while handling signals at frequencies up to 1 GHz. Graphs illustrate such attributes as return losses, delays, and electrical isolation. DM

CIRCLE 949

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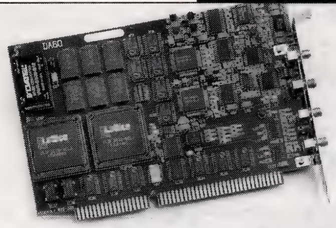

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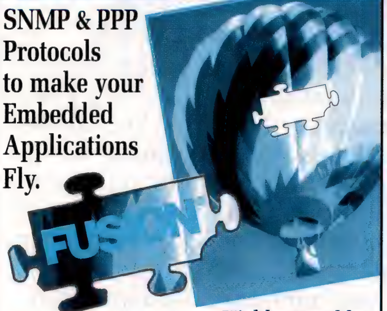

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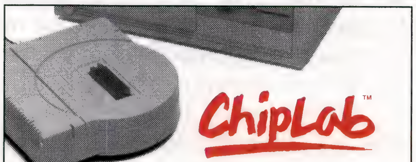

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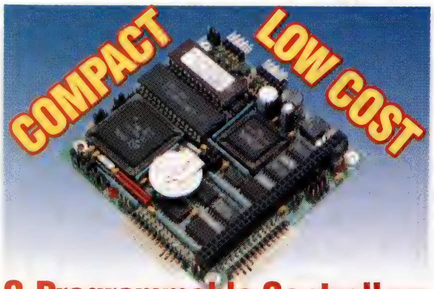

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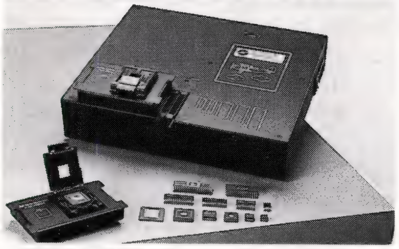

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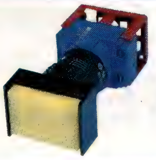

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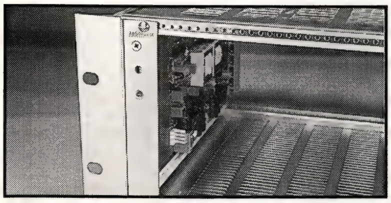

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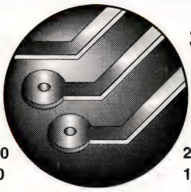

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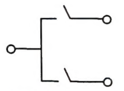

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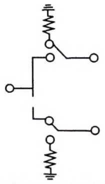

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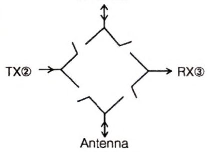

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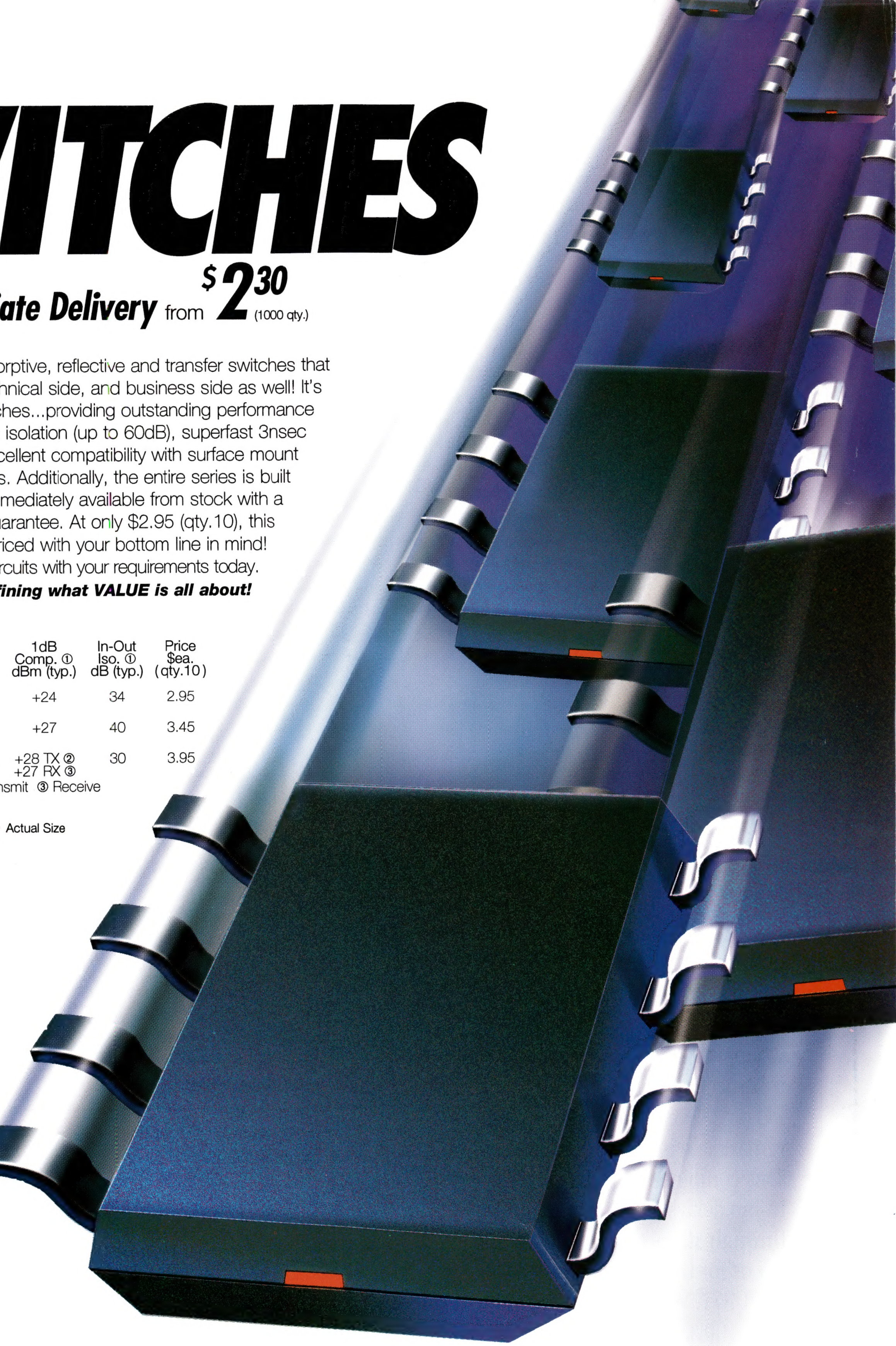

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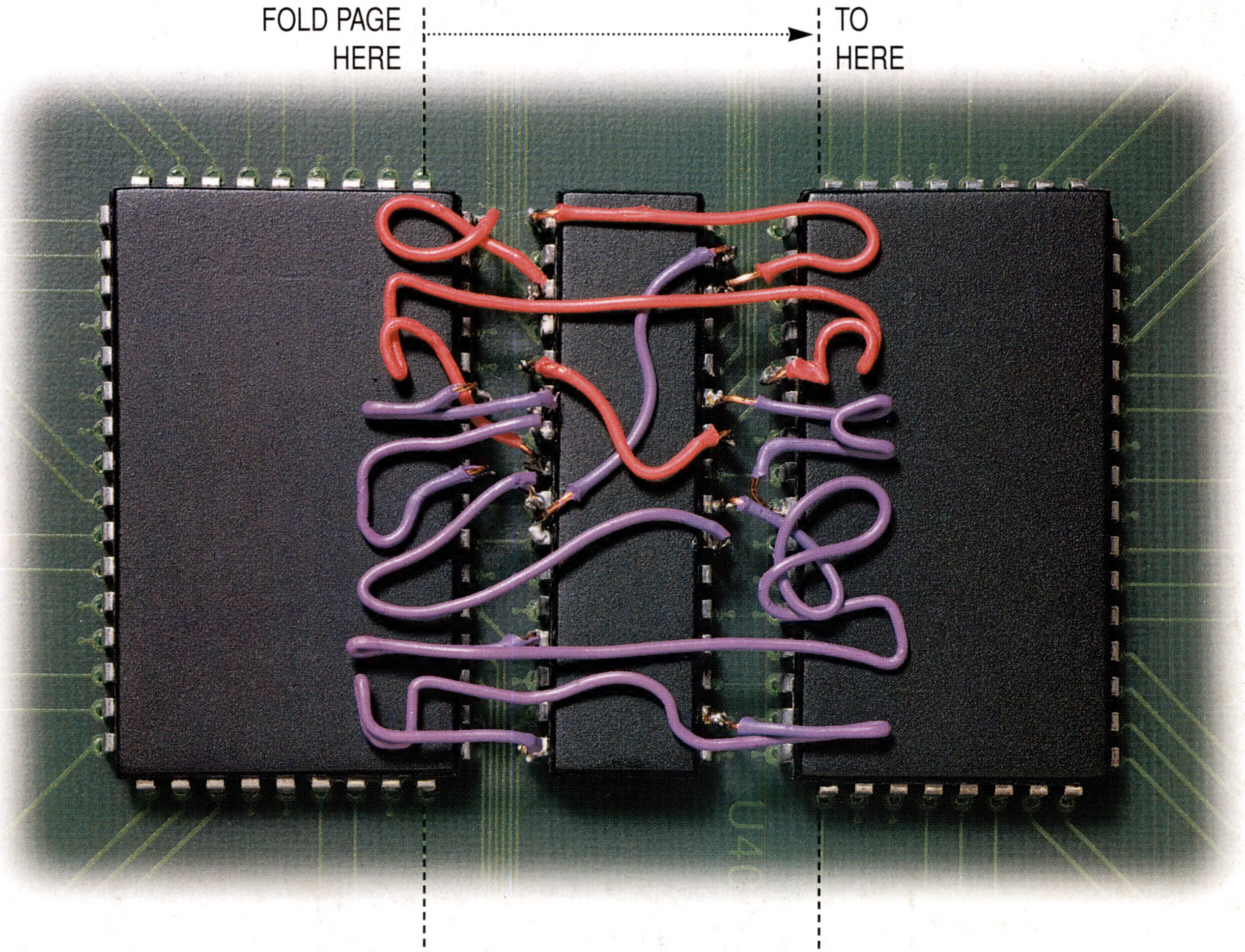

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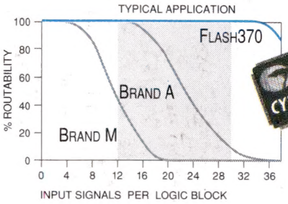
You found it! FLASH370 is a family of seven erasable complex PLDs—with up to a whopping 256 macrocells and 256 I/O pins. Even more remarkable is their 100% routability. This combines with the shortest pin-to-pin delays of any architecture through all speed paths–a blazing 8.5 ns for the 32-macrocell, 44-pin CY7C371. What's more, you get this high speed with 100% timing predictability. So you never have to struggle with variable timing again.



The FLASH370 family's exceptionally clean and simple architecture helps get your products to market faster. And as part of Cypress's comprehensive UltraLogic™ family, the FLASH370 is supported by *Warp*™ VHDL open design tools. So start designing with a data sheet instead of a soldering iron. And watch the competition fold.

Call for your free FLASH370 design kit: *Warp2*™ design tool for the CY7C371, sample certificate and product data. In Europe: (32) 2-652-0270, ext 119*, Dept C312. In Asia: fax your request to 1-415-940-4337*, Dept. C312.

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